Simulation and Optimization of Utility Interactive Photovoltaic Power Generation in Zimbabwe

By

Emanuel Rashayi

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Supervisor: Mr G Gope
Co-Supervisors: Dr E Chikuni
Dr E T Kapuya

This thesis is presented as part of the requirements for the award of the degree of Master of Philosophy in Electrical Engineering, University of Zimbabwe
Declaration

This thesis contains no material which has been accepted for the award of any other degree or diploma in any university. To the best of my knowledge and belief this thesis contains no material previously published by any other person except where due acknowledgement has been made.

Signature:

Date:
Abstract

There is a lot of research being done worldwide in harnessing clean energy, like solar energy and injecting it into existing electricity grids. This project looks at modeling, simulation and optimization of utility interactive PV power generation in Zimbabwe. Considering the abundant sunshine in Zimbabwe and decreasing PV prices on the international market, this can be an option to complement existing power generation from fossil fuels and hydro power stations.

In this thesis the current state of knowledge of single phase grid connected systems was looked at. An Integrated inverter which uses a central transformer was selected as the appropriate system configuration for our environment.

A model of a single phase grid connected Photovoltaic system was developed using MATLAB and SIMULINK. The complete model is made up of smaller models of the photovoltaic panel, the inverter and the load. For the photovoltaic model, the algorithm described by G. Walker [21] was used. For the inverter model, the sinusoidal pulse width modulation algorithm [B1 was used. Two simulations approaches were looked at: one using MATLAB and the other using SIMULINK. There was correlation between the two.

The second phase of the project was to develop a laboratory prototype of single phase grid connected photovoltaic system using inexpensive components which can be sourced locally or in the region.

The SAB80C535 microcontroller was used to realize all the control functions of the inverter. Key parameters which were used in the design of the system included inductor size, power from the photovoltaic panel and the size of the DC capacitor. The inductor size was chosen based on simulation results and the capacitor size was chosen based on 3% ripple [21]. The results of the developed hardware correlated well with the results of the simulations.
In conclusion the research came up with a cost effective inverter for grid connected photovoltaic system. This uses a grid synchronization technique which involves a novel approach of shifting the grid voltage in advance and locking it to the Pulse width modulated voltage from the inverter resulting in power transfer to the grid. A contribution was made towards creation of a PV model Block which can be used in SIMULINK environment. The simulation tool which was developed can be used as a design tool in single phase grid connected systems using a DC source.
Acknowledgements

Firstly, I give God all the glory. Psalms 105:41 says ‘He opened the rock, and the waters gushed out; they ran in the dry places like a river’. Provisions for this research project came from unlikely sources in the most unlikely way!

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Dedicated to Farai Zuriel
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<tr>
<td>A</td>
<td>Diode quality factor</td>
</tr>
<tr>
<td>C</td>
<td>Counting Index</td>
</tr>
<tr>
<td>$f_0$</td>
<td>Fundamental Frequency</td>
</tr>
<tr>
<td>G</td>
<td>Solar irradiation</td>
</tr>
<tr>
<td>Ia</td>
<td>Array current</td>
</tr>
<tr>
<td>Impp</td>
<td>Current at Maximum Power Point</td>
</tr>
<tr>
<td>Iorms</td>
<td>rms value of the output voltage</td>
</tr>
<tr>
<td>Isav</td>
<td>Average value of the supply current</td>
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<td>Isc_T1</td>
<td>Short circuit current per cell at temperature T1</td>
</tr>
<tr>
<td>Isc_T2</td>
<td>Short circuit current per cell at temperature T2</td>
</tr>
<tr>
<td>Isrms</td>
<td>rms value of the supply current</td>
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<td>Ns</td>
<td>Band gap voltage</td>
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<tr>
<td>p</td>
<td>numbers of pulses</td>
</tr>
<tr>
<td>Pin</td>
<td>Input power</td>
</tr>
<tr>
<td>Pin_target</td>
<td>Target input power</td>
</tr>
<tr>
<td>Pout</td>
<td>Output power</td>
</tr>
<tr>
<td>Q</td>
<td>Quadrant of operation</td>
</tr>
<tr>
<td>rsh</td>
<td>Shunt resistance of the solar cell</td>
</tr>
<tr>
<td>Suns</td>
<td>$1 \text{ Sun} = 1000 \text{W/m}^2$</td>
</tr>
<tr>
<td>$T_0$</td>
<td>Period</td>
</tr>
<tr>
<td>T1</td>
<td>25 °C in Kelvin</td>
</tr>
<tr>
<td>T2</td>
<td>75 °C in Kelvin</td>
</tr>
<tr>
<td>TaC</td>
<td>Array Temperature in °C</td>
</tr>
<tr>
<td>TaK</td>
<td>Array working temperature in Kelvin</td>
</tr>
<tr>
<td>Tref</td>
<td>Reference Temperature in °C</td>
</tr>
<tr>
<td>Trk</td>
<td>Reference temperature in Kelvin</td>
</tr>
<tr>
<td>Udc</td>
<td>DC Voltage</td>
</tr>
<tr>
<td>Ug</td>
<td>Grid Voltage</td>
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<tr>
<td>v1rms</td>
<td>The rms Value of the output voltage fundamental component</td>
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<td>Va</td>
<td>Array Voltage</td>
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<td>Vmax</td>
<td>Maximum Voltage</td>
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<tr>
<td>Vmin</td>
<td>Minimum Voltage</td>
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<tr>
<td>Vmpp</td>
<td>Voltage at maximum power point</td>
</tr>
<tr>
<td>Voc_T1</td>
<td>Open circuit voltage per cell at Temperature T1</td>
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<td>Voc_T2</td>
<td>Open circuit voltage per cell at temperature T2</td>
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<tr>
<td>Vorms</td>
<td>rms value of output voltage</td>
</tr>
<tr>
<td>$\eta_E$</td>
<td>European Efficiency</td>
</tr>
<tr>
<td>$\eta_{10%}$</td>
<td>Efficiency at 10% of load</td>
</tr>
</tbody>
</table>
\( \eta_{MPPT} \) Maximum power point tracking efficiency

\( P_{DC} \) Input Power from a DC source

\( P_{\text{m}}, P_{\text{max}} \) Power at MPP

\( \Delta V \) Incremental Voltage

\( \Delta P \) Incremental Power

\( r_s \) Series resistance of the solar cell

\( j_{ph} \) Photo current density in a PV cell

\( j_1 \) Diode current density in a PV cell (one diode model)

\( j_{sh} \) Current density in \( r_{sh} \) of a PV cell

\( j \) Current density

\( k \) Boltzmann constant

\( T \) Temperature in Kelvin

\( q \) Electronic charge

\( j_{01} \) 1\(^{st}\) diode current density in a PV cell (two diode model)

\( V_{o}, u_{out} \) Output voltage

\( j_{02} \) 2\(^{nd}\) diode current density in a PV cell (two diode model)

\( f_s \) Switching frequency

\( \delta_k \) Pulse width of the \( k \)-th pulse

\( \alpha_k \) Position angle of the \( k \)-th pulse

\( \phi, \phi_1, \phi_2 \) phase angle

\( U_{PWM} \) Voltage at the Inverter output

\( X_L \) Inductive Reactance

\( \alpha, \delta_1, \delta_2 \) Load angle

\( p_{\text{loss}} \) Total power losses due to switching in a Power MOSFET

\( p_{\text{sw\_on}} \) Switching loss due to switching ON the Power MOSFET

\( p_{\text{on}} \) On-state losses

\( p_{\text{sw\_off}} \) Switching loss due to switching OFF the Power MOSFET

\( V_F \) On-state voltage

\( r_{DSon} \) Drain-to-source on resistance

\( V_{DD} \) Drain Voltage

\( t_2 - t_1 \) Turn-off delay

\( t_r \) Rise time

\( t_f \) Fall time

\( t_3 - t_2 \) Turn-on delay

\( I_o \) Output current

\( R_g \) Gate resistance
<table>
<thead>
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<th>Description</th>
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</thead>
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<tr>
<td>$C_{gs}$</td>
<td>Gate-to-source capacitance</td>
</tr>
<tr>
<td>$C_{gd}$</td>
<td>Gate-to-drain capacitance</td>
</tr>
<tr>
<td>$g_m$</td>
<td>Transconductance</td>
</tr>
<tr>
<td>$I_g$</td>
<td>Grid current</td>
</tr>
<tr>
<td>$V_{gs}$</td>
<td>Gate to source voltage</td>
</tr>
<tr>
<td>$V_{th}, V_T$</td>
<td>Threshold voltage</td>
</tr>
<tr>
<td>$P_{inv}$</td>
<td>Power from the Inverter</td>
</tr>
<tr>
<td>$P_{grid}, P_g$</td>
<td>Power injected to the grid</td>
</tr>
<tr>
<td>$P_{load}$</td>
<td>Power to the load</td>
</tr>
</tbody>
</table>
### Acronyms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
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<tr>
<td>AC</td>
<td>Alternating current</td>
</tr>
<tr>
<td>BASCOM-8051</td>
<td>BASIC Compiler for the 8051 Microcontroller</td>
</tr>
<tr>
<td>BASIC</td>
<td>Beginners’ All-purpose Symbolic Instruction Code</td>
</tr>
<tr>
<td>C</td>
<td>DC capacitor</td>
</tr>
<tr>
<td>CC1, CC2, CC3</td>
<td>Compare Register 1,2 and 3 of the SAB80C535 microcontroller</td>
</tr>
<tr>
<td>CE</td>
<td>Electromagnetic compatibility</td>
</tr>
<tr>
<td>CO₂</td>
<td>Carbon dioxide</td>
</tr>
<tr>
<td>CRC</td>
<td>Compare Register 0 of the SAB80C535 microcontroller</td>
</tr>
<tr>
<td>CSI</td>
<td>Current source Inverter</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DSM</td>
<td>Demand Side Management</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processor</td>
</tr>
<tr>
<td>DRC</td>
<td>Democratic Republic of Congo</td>
</tr>
<tr>
<td>EU</td>
<td>European Union</td>
</tr>
<tr>
<td>FFT</td>
<td>Fast Fourier Transform</td>
</tr>
<tr>
<td>HF</td>
<td>High Frequency</td>
</tr>
<tr>
<td>IDE</td>
<td>Integrated Development Environment</td>
</tr>
<tr>
<td>IGBTs</td>
<td>Insulated Gate Bipolar Transistors</td>
</tr>
<tr>
<td>IE.5, IE.7</td>
<td>bits in the IEN0 (special function register) for enabling interrupts</td>
</tr>
<tr>
<td>INT4, INT5</td>
<td>External Interrupt 4 &amp; 5 of the SAB80C535</td>
</tr>
<tr>
<td>I-V</td>
<td>Current /Voltage relationship</td>
</tr>
<tr>
<td>LF</td>
<td>Line Frequency</td>
</tr>
<tr>
<td>MATLAB</td>
<td>Matrix Laboratory. A data-manipulation software package</td>
</tr>
<tr>
<td>IE.5</td>
<td>Enables all</td>
</tr>
<tr>
<td>IE.7</td>
<td>IE.5 corresponds to enabling timer2 interrupt and IE.7</td>
</tr>
<tr>
<td></td>
<td>Interrupts on the SAB80C535</td>
</tr>
<tr>
<td>MSX-60</td>
<td>Solarex 60W module</td>
</tr>
<tr>
<td>MTFF</td>
<td>Mean time to First Failure</td>
</tr>
<tr>
<td>m-file</td>
<td>Matlab File</td>
</tr>
<tr>
<td>MOSFETs</td>
<td>Metal Oxide Semiconductor Field Effect Transistors</td>
</tr>
<tr>
<td>MPP</td>
<td>Maximum Power Point</td>
</tr>
<tr>
<td>MPPT</td>
<td>Maximum Power Point Tracking</td>
</tr>
</tbody>
</table>

**m-file**

Matlab File

**MOSFETs**

Metal Oxide Semiconductor Field Effect Transistors

**MPP**

Maximum Power Point

**MPPT**

Maximum Power Point Tracking

**MSX-60**

Solarex 60W module

**MTFF**

Mean time to First Failure
<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1.1, P1.2</td>
<td>pins of Port 1 of the SAB80C535 microcontroller</td>
</tr>
<tr>
<td>P5.1</td>
<td>pin of Port 5 of the SAB80C535 microcontroller</td>
</tr>
<tr>
<td>PCB</td>
<td>printed circuit board</td>
</tr>
<tr>
<td>PV</td>
<td>Photovoltaic</td>
</tr>
<tr>
<td>P-V</td>
<td>Power/Voltage relationship</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width modulation</td>
</tr>
<tr>
<td>SAB80C535</td>
<td>Siemens 80C535 microcontroller</td>
</tr>
<tr>
<td>STC</td>
<td>Standard Test Conditions (G = 1000 W/m², T = 25°C, A.M = 1.5)</td>
</tr>
<tr>
<td>Sw1, Sw3, Sw2, Sw4</td>
<td>Semiconductor switches</td>
</tr>
<tr>
<td>SIMULINK</td>
<td>Block library tool for modeling, simulating and analyzing dynamic systems.</td>
</tr>
<tr>
<td>TCON.5</td>
<td>Timer0 run control bit on the SAB80C535</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
</tr>
<tr>
<td>THDIo</td>
<td>Total Harmonic Distortion of output current</td>
</tr>
<tr>
<td>THDvo</td>
<td>Total Harmonic Distortion of output voltage</td>
</tr>
<tr>
<td>Timer2</td>
<td>Special Function register on the SAB80C535</td>
</tr>
<tr>
<td>UNFCCC</td>
<td>United Nations Framework Convention on Climate Change</td>
</tr>
<tr>
<td>UK</td>
<td>United Kingdom</td>
</tr>
<tr>
<td>USA</td>
<td>United States of America</td>
</tr>
<tr>
<td>VAR</td>
<td>Voltage Ampere Reactive</td>
</tr>
<tr>
<td>VSI</td>
<td>Voltage source Inverter</td>
</tr>
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</table>
CHAPTER 1

INTRODUCTION

Zimbabwe relies on hydropower and coal for its electricity generation. The current generation does not meet demand and about 30% of the total requirements is imported from Zambia, DRC, South Africa and Mozambique [9], [10]. Unlike hydropower, coal poses an environmental threat. Burning of coal results in pollution of the environment. It causes an increase of greenhouse gases, which in turn cause global warming. Global warning has been attributed to the increased content of carbon dioxide. The mainstream view among the scientific community indicates that increased emission of greenhouse gases would lead to a rise in global temperature beyond normal limits [12]. Although recent findings indicate that Africa is not yet a net contributor to the building up of CO₂ in the atmosphere there is need for a review of policy on the use of conventional energy sources, which are not environmentally benign. The United Nations Framework Convention on Climate Change (UNFCCC) and its Kyoto Protocol provide the only international framework for combating climate change. The UNFCCC, the first international measure to address the problem, was adopted in May 1992 and came into force in March 1994. It obliges all its signatories to establish national programmes for reducing greenhouse gas emissions and to submit regular reports, and demands that the industrialized signatory countries, as opposed to developing countries, stabilise their greenhouse gas emissions at 1990 levels. This goal, however, is non-binding. Zimbabwe, a non-Annex I country is a signatory to the Kyoto protocol [27].
Zimbabwe’s position on renewables has been to provide electricity to rural communities, which are far from the national grid. This has gained support from the international community. The donor funded solar projects have seen in excess of 750 kW-installed capacity of solar PV countrywide [10]. Considering that the annual insolation in Zimbabwe is over 2000 kWh/m² [12], which is high by international standards, there is greater need for solar projects to be also done in urban areas through use of grid interconnection. This can remove the use of batteries which have shorter life spans (3 to 5 years). In these systems, power is exported to the national grid which can later be imported back. Though currently not economically viable because of the high cost of PV modules, the figure below shows that PV module prices are expected to be competitive in the future.

**Figure 1.1:** Cost of PV Modules per Watt peak 1976 to 2000 [28]

The insolation profile of PV systems correlates well with load profile of commercial buildings. This can be exploited in Demand side management programmes [9]. This is shown on figure 1.2 overleaf.
Here are some of the benefits which electric utilities can have as a result of Grid interconnection of PV systems:

- Reduced transmission, distribution losses
- Control of distribution line voltage
- Reduced reactor or capacitor equipment
- Power factor / VAR control

1.1 Thesis Objectives

Specific objectives of this thesis can be summarized as follows:

- To develop a model of a Micro-PV Power Generation system using MATLAB
- To perform simulation studies so as to determine parameters needed to optimize transfer of power from solar panels to the grid under different environmental conditions
• To design and develop a prototype of a PV - grid interconnection system
• Experimentation with the developed prototype so as to validate the model developed in MATLAB.

1.2 Thesis Organization

This thesis is essentially divided into two parts. The first part comprises of Chapter 2 which looks at general information on single phase grid-connected PV systems. The second part (Chapters 3-7) provides specific information on a single phase grid-connected PV system. The individual content of each chapter and its corresponding appendix is outlined below.

Chapter 2 presents an up-to-date and orderly review of the state of knowledge of single phase grid interconnected PV systems and explores various inverter technologies being used to provide interface between these PV systems and the national electric grid.

Chapter 3 presents modeling and simulation of a Micro-PV Power station using MATLAB. Firstly a model of the PV system is created using the MATLAB Language. SIMULINK is used to design a customized PV block function. Other models which constitute the single phase grid connected system are taken from the Simpower systems Toolbox.

Chapter 4 presents the Hardware design of the proposed system. The design uses the development system in Appendix C.4. It is supported by simulations done using MATLAB codes in Appendix B. The components used in the design are documented in Appendix C.
Chapter 5 presents the software design of the proposed system. Various software algorithms are looked at. Software routines are developed using BASCOM-8051 and are documented in Appendix E.1.

Chapter 6 presents the results of experimentation with the developed prototype. This is compared with results obtained from simulations.

Chapter 7 summarises, concludes and gives an outlook for future work.
Chapter 2

Literature Review

2.1 Introduction

This chapter looks at the state of knowledge of grid connected PV systems. It explores the characterisation of inverters for grid connected PV systems and also looks at the various systems configuration. Advantages and disadvantages of each system are discussed. The chapter concludes with a discussion on PV utilisation programmes around the world.

2.2 Single Phase Grid Connected PV System

Figure 2.1 shows the topology of a single phase grid connected PV system. The PV array is invariably a DC current source. The Inverter stage converts DC voltage to AC voltage. The filter stage reduces the harmonic content of the inverter output current. For power to flow from the PV array to the national grid, the voltage from the PV system must always be higher than that of the grid supply. The current from the PV system inverter should be synchronised with the voltage of the grid supply, to allow power flow at unity power factor.

![Figure 2.1: Single Phase Grid Connected PV system](image)

Figure 2.1: Single Phase Grid Connected PV system
2.3 Characterization of PV inverters.

Inverters are a key component in the production of electricity with grid connected PV systems. Cost must be reduced and efficiency must be increased. These are two of the main priorities if PV systems are to maximize their potential in carbon-free energy generation.

Inverters for PV systems are characterized by the following:

- DC-AC conversion efficiency
- Cost
- Total Harmonic Distortion (THD) and Power Factor
- Maximum Power Point Tracking (MPPT) efficiency
- DC current injection
- Mean time to first failure (MTFF)
- Islanding Prevention

2.3.1 DC-AC Conversion efficiency

The DC-AC electrical conversion efficiency is the most important parameter for grid connected PV power generation and the process is representative of different inverters. Efficiency of inverters varies with load. In Europe they have come up with a normalized efficiency, usually known as European Efficiency, \( \eta_E \) [1], [2]. It is defined as the function of the efficiency at the defined percentage values for nominal AC power. This is shown in the following equation.

\[
\eta_E = 0.03 \eta_{5\%} + 0.06 \eta_{10\%} + 0.13 \eta_{20\%} + 0.1 \eta_{30\%} + 0.48 \eta_{50\%} + 0.2 \eta_{100\%} \quad \text{eq 2.1}
\]
As an example, where this equation has $\eta_{10\%}$, it represents the efficiency at 10% of the nominal inverter power. This can be obtained by varying the input power and then measuring the output power. $\eta_E$ is an appropriate way of describing efficiency for fixed (i.e. non-tracking) PV systems. Efficiencies of around 94% have been recorded for transformerless inverters in Europe [1], [2], [3].

2.3.2 Cost per watt of PV inverters

The cost per watt of PV inverters varies depending with the technology used in the design of the PV inverter. Transformerless topologies have a low cost per watt as they do not use the Line Frequency (LF) transformer. The trend has been to reduce the cost/efficiency ratio. However they are technical challenges faced in reducing cost per watt of PV inverters. Eliminating the use of LF transformers creates a galvanic connection between the inverter and the grid. Other methods are needed to avoid DC current injection into the grid. With current designs of PV inverters for grid connection, the inverter represents around 16% of the cost of PV installations with a nominal power below 5 kW. For Large-scale PV plants it is around 10% [1].

2.3.3 Maximum Power Point Tracking (MPPT) Efficiency

The DC power input to an inverter depends on which point in the current-voltage ($I-V$) curve the PV array is working at. Ideally, the inverter should operate at the maximum power point (MPP) of the PV array. The MPP is variable throughout the day, mainly as a function of the environmental conditions such as irradiance and temperature, but inverters directly connected to PV arrays have an MPP tracking algorithm to maximize energy
transfer. The MPP tracking efficiency, $\eta_{\text{MPPT}}$, can be defined as the ratio of the energy obtained by the inverter from a PV array, to the energy obtained with ideal MPP tracking over a defined period of time. This is defined in the equation overleaf:

$$\eta_{\text{MPPT}} = \frac{\int_0^t P_{\text{DC}} \, dt}{\int_0^t P_m \, dt} \quad \text{eq 2.2}$$

Where $P_{\text{DC}}$ is the DC input power to the inverter and $P_m$ is the ideal MPP.

Many tracking algorithms have been proposed based on amongst other parameters, incremental conductance, incremental perturbation of voltage, parasitic capacitance, constant voltage, voltage with temperature correction and fuzzy logic control [5], [19], [20].

Nevertheless the ‘perturb and observe’ based algorithms are in practice the most commonly used, due to the ease of implementation. Such algorithms are based on a perturbation of a PV array’s operating voltage by a small increment, $\Delta V$, after particular intervals of time and the resulting change in power, $\Delta P$, is measured. If $\Delta P$ is positive, the next incremental perturbation of voltage is positive; if $\Delta P$ is negative, the next incremental perturbation is negative. Nevertheless, this algorithm can have some limitations, and these can reduce the MPP tracking efficiency in certain operating conditions. At very low levels of irradiance e.g. during sunrise and sunset – the power curve becomes very flat and makes it very difficult to distinguish the true location of the MPP. Another factor is the impossibility of defining the exact MPP, since the inverter $\Delta P$ oscillates around this point. The tracking Algorithm can exhibit erratic behaviour under rapidly changing irradiance levels. Partial shadowing can also influence MPP
tracking behaviour, but this problem can be overcome by using different times for perturbation, as a function of the power variation in time or by performing alternate voltage perturbations.

2.3.4 Total Harmonic Distortion (THD) and Power Factor

The total harmonic distortion, THD, of the current generated by the PV inverter is regulated by international standard IEC61000-3-2, UL 1741. This is shown in Table 1 and Table 2. Electromagnetic compatibility and ‘CE’ marking is regulated by the EU directives 89/336/CEE and 93/68/CEE. [3]

Inverters for grid connected PV systems must have a defined power quality, The standards referred to above require a THD of \( \leq 5\% \) for the harmonic spectra of the current waveform (measured up to harmonic number 49) while the THD of the voltage should be lower than 2%. The AC power operation level for which this requirement must be fulfilled is not actually mentioned, so it is generally considered to be the nominal power. Inverters THD output current increases at power levels below nominal. The power factor is also related to the quality of the generated energy. Ideally it should be unity.

<table>
<thead>
<tr>
<th>Current Harmonic</th>
<th>Percentage of Fundamental (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-9</td>
<td>4</td>
</tr>
<tr>
<td>11-15</td>
<td>2</td>
</tr>
<tr>
<td>17-21</td>
<td>1.5</td>
</tr>
<tr>
<td>23-33</td>
<td>0.6</td>
</tr>
<tr>
<td>33-49</td>
<td>0.3</td>
</tr>
<tr>
<td>Even order</td>
<td>25% equivalent odd harmonics</td>
</tr>
</tbody>
</table>

Table 2.1: Permissible Harmonic current limits at full load, Australian Draft Standard and UL 1741 [3]
### Table 2.2: Permissible Harmonic current limits, Europe (IEC 61000-3-2) [3]

<table>
<thead>
<tr>
<th>Current Harmonic (order = n)</th>
<th>Maximum permissible harmonic current (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2^{nd}</td>
<td>1.08</td>
</tr>
<tr>
<td>3^{rd}</td>
<td>2.3</td>
</tr>
<tr>
<td>4^{th}</td>
<td>0.43</td>
</tr>
<tr>
<td>5^{th}</td>
<td>1.14</td>
</tr>
<tr>
<td>6^{th}</td>
<td>0.30</td>
</tr>
<tr>
<td>7^{th}</td>
<td>0.77</td>
</tr>
<tr>
<td>8^{th} &lt; n &lt; 40^{th}</td>
<td>0.23(8/n)</td>
</tr>
<tr>
<td>9^{th}</td>
<td>0.4</td>
</tr>
<tr>
<td>11^{th}</td>
<td>0.33</td>
</tr>
<tr>
<td>13^{th}</td>
<td>0.21</td>
</tr>
<tr>
<td>15^{th} &lt; n &lt; 39^{th}</td>
<td>0.15(15/n)</td>
</tr>
</tbody>
</table>

#### 2.3.5 DC Current Injection

The THD of the generated current’s waveforms is related to DC current injection into the electrical grid via the PV inverters. The adverse effect of DC injection into the general grid by customers can shift the mains transformers’ operating point towards possible saturation, which might result in high primary current that could trip the fuses and thus cause a power outage to that section of the network. Transformers lifetime and efficiency may also be reduced, while DC causes cathodic corrosion of the cabling [26].

#### 2.3.6 Islanding Prevention

Islanding is the electrical phenomenon that occurs in a section of a power network disconnected from the main supply where the loads in a neighborhood are entirely powered by the PV system. Islanding is undesirable in terms of public safety and that of the electricity distributor’s staff, the quality of supply and possible damage to equipment in the event of the automatic or manual reconnection of the distribution system to a power island. Islanding prevention is therefore also usually included in the inverter.
2.3.7 Mean –Time-to-First Failure (MTFF)

The mean time to first failure, MTFF of an inverter should theoretically be about 50 years, provided it is not exposed to excessive temperature. However values have been reported in the range of 5-10 years [26], a shorter lifespan than other major PV system components, which are designed to operate in excess of 20 years. Further efforts should be made by inverter manufacturers to increase the MTFF.

2.4 Current System Configurations

The system configuration depends on the inverter type. Early inverters were mainly central with rated power above 1 kW. These inverters were line commutated. They used either High Frequency (HF) or Line Frequency (LF) transformers for galvanic separation and stepping up of voltage. Later self commutated inverters appeared on the market. These use Pulse Width Modulation (PWM) techniques. The various system configurations are given in subsequent sections.

2.4.1 Plant Oriented System Configuration

This system uses central inverters as shown in figure 2.2. The advantage of this system is that it is robust, highly efficient and has low cost per watt. However they are inherent problems with this configuration. These are as follows:

- poor power factor (between 0.6 and 0.7)
- bulky, need special filters for compensation
- high harmonic content.
- need for DC wiring which increases system costs
- safety concerns
- the system is not expandable as the central inverter rating limits the panels required
• the system is not fault tolerant

![Diagram of Plant Oriented System Configuration](image)

**Figure 2.2:** Plant Oriented system configuration [7]

### 2.4.2 Module-Oriented System Configuration

This system uses module-oriented inverters. These can be string inverters or multistring inverters [4]. Several modules would be connected in series on the DC side. The inverter power can be up to $2\ kW$. Nominal power of the system can be extended to several MWp. The system is shown in figure 2.3. In this system, losses due to mismatch and shading are reduced. There is a high degree of fault tolerance. If one inverter fails the system will remain functional. However the cost per watt is higher than for the plant-oriented system.

![Diagram of Module Oriented System Configuration](image)

**Figure 2.3:** Module Oriented System Configuration [7]
2.4.3 Module Integrated System Configuration

This system uses module-integrated inverters. In a module-integrated system, each PV module has its own inverter. See figure 2.4. The power ranges from $50\, W$ to about $500\, W$.

![Figure 2.4: Module Integrated System Configuration [7]](image)

The parallel connection is on the AC side. There is no DC wiring in this system. The main concern in this system is lack of central control of the complete system. Also the unit cost per watt is high for this system.

Some of the advantages of Module integrated system configuration are:

- Each module works independently: if one fails, the other AC modules will keep delivering power to the grid.
- High modularity allowing easy system expansion.
- Low minimum system size of one AC module, lowering the threshold for individuals to start their own PV plant.
- Use of standard AC installation material, which reduces costs of installation material and system design.
- Low conduction losses and cable costs.
- No mismatch losses at system level as each AC module operates in its own Maximum Power Point (MPP).

2.5 Inverter Topologies

The different commercially available PV inverter topologies for single phase grid connected systems are shown in figure 2.5.

![Diagram of PV inverter topologies](image)

Figure 2.5: Different commercially available PV inverter topologies for Single-phase grid connected PV systems [2], [3]

2.5.1 Transformer Based Inverter Topologies

Transformer based inverter topologies use either a high frequency transformer or a line frequency transformer. High frequency transformer based topologies reduce the physical size and cost of magnetic components. The topology is shown in figure 2.6. In order to reduce the switching losses on the high voltage side, the push-pull converter boosts the voltage to grid level and shapes the current waveform as well. A full bridge switched at line frequency is used in a second converter stage as an unfolding/inverting stage.
Figure 2.6: PV inverter with several conversion stages and high frequency transformer

Two converters in series reduce the efficiency and make the control more complex. Other transformer based topologies are shown in figure 2.7(a) overleaf. The transformer steps up the voltage to grid level. The transformer also provides galvanic isolation of the PV module from the grid. Use of the transformer increases the system costs and lowers the efficiency of the inverter. Also the weight of the inverter increases. The inverter shown in figure 2.7(b) overleaf is available on the American market.

The inverter consists of three conventional single phase full bridges each with their mid points connected to the primary winding of a transformer. The secondary windings of the transformers are connected in series and the turns ratios of the transformers are chosen as multiples of each other.
Figure 2.7: Inverters with line frequency transformer, (a) Self commutated full bridge (b) Magnetic coupled [6]

Generally, an inverter of this type having $n$ primary transformer windings is capable of generating $3^n$ combinations of different voltages across the secondary transformer windings and synthesizes the sine wave by means of a stepped waveform (not by means of PWM) [6]. The advantage of the topology is the relatively accurate replica of a sine wave accomplished with low switching frequencies and a cheap and robust full-bridge. The major drawback is its bulkiness.
2.5.2 Transformerless Inverter Topologies

Avoiding the use of the transformer in inverter topologies has been seen to increase the efficiency of the inverter by 1-3 % [2], [3], [5]. Also the cost, size, weight and complexity of the inverter goes down. Figure 2.8 overleaf shows the topologies. However avoiding a transformer in PV inverter topologies results in a galvanic connection of the grid and PV array. Some countries such as Italy and UK require topologies with a transformer.

For systems with High DC voltages, that is, use of many PV modules with cells connected in series, topologies in Figure 2.8 (a) and (b) will be appropriate.

If one uses low DC voltages there will be a need for boosting the voltage to grid level. This can be realised by the topology in figure 2.8 (c). The use of many conversion stages lowers the efficiency of the inverter. The boosting of the voltage is limited to 4-5 times.

While using a boost converter to boost the low PV voltage, shaping and inverting of the output current have to be done in the second converter stage at high voltage level.
Figure 2.8: Transformerless PV inverters (a) PV inverter with several conversion stages including a boost stage (b) step down (c) line commutated [3]
2.6 Switching Devices

Early inverters used thyristors for switching. However as the inverter technology for grid connected PV systems developed, the switching devices that became common were MOSFETS (Metal Oxide Semiconductor Field Effect Transistors) and IGBTs (Insulated Gate Bipolar Transistors). Today, most commonly used switching devices in self-commutated inverters are MOSFETs for inverters with DC voltage ratings below 300V for various power ratings. IGBTs are generally used for inverters with DC voltage ratings above 300V. The switching frequencies range from 16-32 kHz for MOSFETs and from 18-20 kHz for IGBTs. Figure 2.9 shows the different transistors used at different power ranges. Recent switching device developments may further influence PV inverter designs.

The new MOSFETs CoolMOS available on the market up to 800V has significantly lower $R_{DSon}$ and gate capacitance. This allows for more efficient and cheaper DC to AC conversion [1].

![Figure 2.9: Different transistors used at different power ranges [29]](image)

For low power and low voltage applications, the preferred switch is the MOSFET. The MOSFET has very low conducting losses ($R_{DSon}$ of 8 mΩ available for 55 V, 100 A transistors) and is also easy to control which gives low switching losses. Additionally, it
has a parasitic anti-parallel diode that can be used as a freewheel-diode. If this diode
gives poor performance (long reverse recovery time or high forward conducting voltage)
external diodes, preferably Schottky diodes could be used in parallel.

2.7 PV Utilisation Programmes around the World

The information in this section was taken from the internet [22-26]. It reviews PV
development programs in USA, Japan, Europe, India and Australia.

2.7.1 USA

In the 1970’s and 1980’s, the U.S Department of Energy (DOE) monitored household
loads in one of their research programs. They evaluated and provided technical
information on residential PV systems in different regions; built and monitored PV
powered homes and commercial buildings, and studied their impacts on the power
distribution network. This program is now superceded by the “Solar 2000” program,
which aims to develop economically competitive PV systems and hence increase
installed capacity in the US from less than 50 MW in 1991 to 200-1,000 MW by 1995-
2000 and 10,000-50,000 MW by 2010-2030.

Other US programs include the Utility PV Group (UPVG). They planned to educate
utility end users as to the value of PV in their systems and introduced a cost effective and
emerging PV technology in US Utility grids from 1993 onwards.

The National Renewable Energy Laboratory’s PV: BONUS program includes support for
PVs used in roofing, windows, domestic and commercial buildings and in kit homes for
off-grid sites.

Currently there are on-going PV projects in the US. In the states of Colorado and Texas,
for example, residents and business owners are encouraged to install a PV system to meet
with their energy demands. They were informed of the advantages of incorporating the PV modules on their rooftop and building.

### 2.7.2 Japan

The Japanese “Sunshine Project” started in 1974. Since then, they have moved rapidly from R&D to widespread PV application. They have been emphasizing on utility connected systems, particularly residential rooftop systems, which minimizes land use. Testing has been done since 1989 and their goal is to have 1 million 200 kWp systems by 2010. Guidelines for utility connection, including one on the use of one pricing structure, are now in place. A generous 2/3-subsidy scheme for 1000 rooftop systems is also under development.

Grid connected market in Japan increased satisfactorily in 2001. 50 kW for off-grid domestic application, 5960 kW for off-grid non-domestic application, and 116,000 kW for grid-connected distributed applications, especially in residential sector were installed. In year 2000, grid-connected distributed systems increased dramatically because the additional budget for Residential PV system Dissemination Program was approved to correspond to great demand for residential PV systems. In this connection, the total installed capacity of grid-connected distributed systems in 2000 increased 77% from the previous year.

### 2.7.3 Europe

Switzerland has a PV program stemming from a 10-year moratorium on nuclear power. Their R&D program was developed in 1987, followed by testing of a 3 kW prototype system. In 1988 ten 3 kW PV systems, using a specially designed 3 kW high efficiency inverter were installed. A one to one buying and selling cost for the electricity used
produced by households has been arranged with the utility. By the year 1990, 100 of such systems had been installed.

The Swiss wanted to reduce PV land use requirements; therefore, a 100 $kW$ array was installed along a motorway sound barrier that is an ingenious way in providing a visible demonstration of the technology.

In 1992, Austria began a “200 $kW$ Photovoltaic Rooftop program”. Financial support is provided to the householder for the building integrated, utility connected PV systems up to 3.6 $ kWp$. The program was closely monitored to assess the feasibility of decentralized generation.

In the last several years, Germany has executed important programs in the field of PV that have triggered remarkable results in the market development and technology progress. Complementary to the R&D program, new PV-funding sources with growing importance, mainly in the area of market introduction have been established:

- The “Electricity Feed Law,” introduced in 1991, was replaced by the “Renewable Energy Law”, in April 2000. The new Law rules the input and favorable payment of electricity from renewable energies by utilities. For PV systems built before the end of 2001, a feed in tariff of 0.51 EUR/$kWh$ will be paid.

- In January 1999, the Federal Ministry of Economics and Technology (BMWi) started the “100000 Rooftops Solar Power Program”. Until November 2001, almost 37500 applications were received and a total capacity of 126 $ MWp$ was granted. The program is a soft loan program (current rate of interest 1.9% per year) and lasted until 2003. Applications can be submitted by small and medium
enterprises as well as by individuals. The BMWi offered a budget of approx. 460 million EUR for the whole period of this program.

- Moreover, the BMWi supports the application of renewable energies (solar-thermal, geothermal, biomass, etc) with soft loans or subsidies. The PV initiative, “Sun at School”, is part of this program.

- Some of the Federal states (Lander) have defined their own programs, mainly to support the application of renewable energy and energy conservation.

- The Federal German Environmental Foundation (DBU) supports development and demonstration in the field of renewable energy sources and energy conservation.

- A number of utilities have launched initiatives to build PV-demonstration and pilot systems or to provide advice and information. In a growing number of cases, financial support for the national use of energy and for renewable energies is provided. Cost–effective payments for every kilowatt-hour of energy fed into the public grid from PV and other renewable energy systems are offered by some utilities belonging to cities and communities.

2.7.4 India

While most developing countries install stand-alone PV systems, India has planned major PV programs, including grid-connected systems up to 100 $kWp$. A 100 $kWp$ is already installed in Kalyanpur, at a cost of US$ 1.5 m. Seventy central village sized PV Plants, ranging from 2 to 10 $kW$ are now in operation. In 1993-94 a further 200 $kW$ of the same system was installed. India also has plans for a 2 $MW$ grid connected plant, to increase PV production volume and reducing costs.
2.7.5 Australia

PV cell and module production levels for Australia fell slightly in 2000, due to the disruption in production caused by the merger and factory relocations of BP Solar and Solarex. This has contributed to an increase in imports of cells and modules. Although not operating in the Australian usage figures, there has also been an increase in imports of modules, which are subsequently re-exported in complete systems. Approximately 50% of local production was also exported.

Installed PV capacity in Australia grew by 15% in 2000, with 3.89 MWp PV system installed. A large proportion (over 80%) of this was for installations on residential, commercial and educational buildings, a market stimulated by an Australian Government PV rebate program. PV used in the Sydney Olympic site and on service stations also contributed to this market area. This was offset by decrease use in the off-grid industrial market, which has previously dominated Australian sales. The Telecommunications market has been disrupted by an outsourcing of off-grid power supply installations and maintenance and by some saturation of that market sector.

The grid-connected PV market continues to grow and now represents 10% of installed capacity. The significant use of PV in the Sydney Olympic site has contributed to this increase, as have various utility green – power programs and the Australian government’s PV rebate program.

Australian companies are active in the international PV market, both as suppliers of equipment and of services related to PV system design, installation, monitoring, maintenance and training.
2.8 Future of Grid –connected PV systems

Although photovoltaic may not currently have good pay back period, this does not imply that they should not be implemented today. PV works regardless of the economic effects, and is a viable energy supplement. By building systems today, the knowledge and experience gained from their operation can be applied to improve future use. Additionally, many things in which people invest their money today never pay back. For example, automobiles do not pay back, but that does not make them any less of a necessity or prevent people from purchasing them. Photovoltaics may become necessary in the future, and this would cause economics of a system to become a secondary factor in deciding whether or not to purchase one.

The implementation of a large-scale or bulky power generation depends on PV’s performance, cost, value and corporate support. The performance of PV can now be estimated with considerable certainty based on data that was collected in various experimental projects.

PV module costs have declined in recent years but there is no hard evidence that its cost can compete with conventional power sources. To make PV the ultimate in renewable source in utility grid systems, the costs must decline further. Newer materials, production processes and production volume will assist in lowering the cost of PV modules and so will partnership among the manufacturers and R&D organizations. The government can also help promote the use of grid – connected PV systems and subsidize the cost of the PV system.
Chapter 3

Micro-PV Power Station Modeling and Simulation

3.1 Introduction

The thrust in this chapter is to come up with a model of a single phase grid-connected PV system. Invariably this is composed of smaller models: PV model, MPPT model, Inverter Model, Load Model and Grid Model. The modeling starts with the realisation of a mathematical model of a PV module. A lot of modeling software exists on the market. Usage of these modeling tools depends on the cost, flexibility and application. All the models and the complete model were developed using MATLAB. MATLAB is a high-level technical computing language and interactive environment for algorithm development, data visualization, data analysis, and numerical computation. Using MATLAB, you can solve technical computing problems faster than with traditional programming languages, such as C, C++, and Fortran. Within the MATLAB environment one can also choose to use SIMULINK which uses Block programming. The PV model is validated using information provided in data sheets by manufacturers. An MSX-60 solar panel was used for this purpose [17].

3.2 Model of a Single Phase Grid-connected PV System

Figure 3.1 shows the complete model of a single phase grid-connected PV system. This model will be used to carry out simulation studies of single phase grid connected PV systems. Power quality from the system will be studied. The effect of various parameters on the harmonics produced by the system can be studied. This, if validated by a hardware
realization, (which is going to be carried out in the next phase of the research project),
can be used as a design tool.

![Figure 3.1](image)

**Figure 3.1:** Model of a Single Phase Grid Connected PV system

3.3 PV modeling

3.3.1 Cells, Modules, Panels and Arrays

A conventional solar cell consists of a wafer of silicon that is 0.5 mm thick. Typical cells
that are 100 mm in diameter produce about 1 W and are grouped into modules, of dozens
of cells. Modules are further grouped into panels and then arrays, which may produce
power up to several kilowatts

3.3.2 Solar Cell Models

The simplest solar cell can be represented by a diode in parallel with a constant current
source. However, for practical cells, imperfections in devices must be taken into account.
A practical device has leakage current modeled by a shunt resistance (r_{sh}). When a cell is
loaded, it is found that a certain voltage is dropped within the cell. This is represented by
a series resistance, r_s. The resulting model is shown in figure 3.2 [B2]
Using Kirchoff’s nodal equation for the above model:

\[ j_{ph} = j_1 + j_{sh} + j \]  \hspace{1cm} eq 3.1

from which:

\[ j = j_{ph} - j_1 - j_{sh} \]

Using Shockley diode equation

\[ j_1 = j_0 \exp \left( \frac{q(V_o + j r_s)}{\alpha k T} \right) - 1 \]  \hspace{1cm} eq 3.2

and

\[ j_{sh} = \frac{V_o + j r_s}{r_s} \]  \hspace{1cm} eq 3.3

results:

\[ j = j_{ph} - j_0 \exp \left( \frac{q(V_o + j r_s)}{\alpha k T} \right) - 1 \] - \frac{V_o + j r_s}{r_{sh}} \]  \hspace{1cm} eq 3.4

Solar Cells can also be represented with a two diode model shown in figure 3.3
Such a two diode model can again be analyzed starting from Kirchoff’s nodal theorem:

\[ j = j_{ph} - j_{01} - j_{02} - j_{sh} \] ………………………………………………………….eq 3.5

from which:

\[ j = j_{ph} - j_{01}\{\exp\left(\frac{q(v_0 + j r_s)}{\alpha k T}\right) - 1}\} - j_{02}\{\exp\left(\frac{q(v_0 + j r_s)}{\beta k T}\right) - 1}\} - \frac{v_0 + j r_s}{r_{sh}} \] 

…..eq 3.6

Though the two diode model for a PV cell is known to yield superior approximation results compared to the one diode model, the PV model in this project was developed in MATLAB using the following simplified model.
For the computation of the PV model, the one described by G. Walker [21] is used. The model is developed using Solarex MSX60 Solar panel. The MSX60 PV model is shown in figure 3.5

**Figure 3.5:** MSX60 PV Model

**Inputs**

1. *Array Voltage (Va)*

2. *Irradiation (number of Suns, 1 Sun = 1000 W/m²) , (G)*

3. *Array Temperature in °C (TaC)*

**Constants**

1. *Diode quality factor (A)*

2. *Band gap voltage(Vg)*

3. *Number of series connected cells(Ns)*

4. *25 °C in Kelvin(T1)*

5. *Open circuit voltage per cell at Temperature T1(Voc_T1)*

6. *Short circuit current per cell at temperature T1(Isc_T1)*

7. *75 °C in Kelvin(T2)*
8. Open circuit voltage per cell at temperature T2 (Voc\_T2)

9. Short circuit current per cell at temperature T2 (Isc\_T2)

10. Array working temperature in Kelvin (TaK)

11. Reference Temperature in °C (Tref)

12. Reference temperature in Kelvin (Trk)

Output

1 Array current (Ia)

3.3.3 MATLAB Simulation of the MSX60 PV model

An *m*-file of the MSX60 PV model is documented in Appendix A. The relationships of inputs, constants and the output is defined in the Appendix. In order to make use of this PV model, it has to be simulated to determine the *I-V* characteristics at different conditions. Validation of this model is done by comparing the *I-V* characteristics with the one provided in the manufacturer’s datasheets.

Figure 3.6 shows the *I-V* characteristics of the MSX60 PV model under the following conditions:

- G = 1000 W/m²
- Air mass = 1.5
- Temperature is varied from 0 °C to 75 °C in steps of 25 °C
Figure 3.6: $I$-$V$ Characteristics of the MSX60 PV model under different temperature values

Figure 3.7 shows the $I$-$V$ characteristics of the MSX60 PV model under varying Irradiation values and at a fixed temperature of 25 °C.
To compare the $I$-$V$ characteristics of the model with the one in the manufacturer’s datasheets, the results in the datasheets were exported into the MATLAB workspace. Figure 3.8 shows a close match between the information in the datasheets and the simulated model.
3.3.4 PV Simulink Block

Simulink provides the flexibility in modeling and simulation of systems by making use of
blocks. One can drag and interconnect simulink blocks including even customized blocks
like the PV block which was developed by making use of the embedded Matlab function
block.

![Figure 3.9: PV Model Simulink Block](image)
3.4 MPPT Model

Maximum power point is the point on the $I-V$ characteristic curve of a solar cell where power is maximum. This can be seen in figure 3.10 which shows the $P-V$ characteristics of the MSX60 PV model under standard conditions. $P_{\text{max}}$ is the maximum power of the module which is 60 W under standard conditions.

![MSX-60 P-V Characteristics at G=1000W/m² and T=25 degC](image)

**Figure 3.10:** $P-V$ characteristics of the MSX60 PV model under standard conditions

The MPPT model determines the output current and voltage of MSX60 PV model which will give $P_{\text{max}}$ under different operating conditions. This will ensure extraction of maximum power from the PV model under all operating conditions. Figure 3.11 illustrates the parameters used in the MPPT model.
The *m-file* for the MPPT model is documented in Appendix B. Also the Simulink version of the MPPT model was developed (*see figure 3.12*). To test the model, the simulation was done using the standard conditions i.e. $G = 1000 \ W/m^2$, $T = 25 ^\circ C$, Air mass = 1.5. Results obtained are shown in table 3.1. These are compared with the ones from Data sheets.

<table>
<thead>
<tr>
<th></th>
<th>Voltage (Vmpp)/V</th>
<th>Current (Impp)/A</th>
<th>Power (Pmax)/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>From Matlab simulation</td>
<td>17.02</td>
<td>3.55</td>
<td>60.4</td>
</tr>
<tr>
<td>From Manufacturer’s data sheets</td>
<td>17.1</td>
<td>3.5</td>
<td>60</td>
</tr>
</tbody>
</table>

**Table 3.1:** Validating the MPPT model

**Figure 3.11:** MPPT Model

**Figure 3.12:** MPPT model Simulink Block
3.5 Inverter Model

A PV array produces DC power and before it can be connected to the grid which produces AC power, it must be converted to AC power. The DC power is converted to AC power using an Inverter. The following parameters are important in the development of the Inverter Model.

- Efficiency of the inverter
- Power quality

The Inverter Model was developed using a Sine-PWM inverter. This is a very popular inverter. It uses \( p \) pulses per half period \( (T/2) \) of the desired sinusoidal waveform of the

---

**Figure 3.13:** MPPT using Simulink Blocks (inside the MPPT block)
output voltage. The pulse width of these pulses varies sinusoidally over the half period $T_0/2$. The switching frequency is $2p$ times the desired frequency $f_0$:

$$f_s = 2p \, f_0$$  \hspace{1cm} \text{eq 3.7}$$

These pulses may be unipolar (0 to $V_s$) or bipolar (-$V_s$ to +$V_s$). The following section will discuss the unipolar pulses.

### 3.5.1 Sine-PWM inverter using unipolar switching

The unipolar Sine-PWM inverter output may be considered as the summation of $p$ pulse waveforms where each pulse has a positive and negative pulse over the period $T_0$.

Consider one such $k$-th pulse waveform with a pulse width $\delta_k$ and the position angle $\alpha_k$ with respect to the beginning of the period $T_0$ and where [B1]:

$$\alpha_k = (2k - 1) \frac{\pi}{2p} \quad \text{and} \quad 0 < \delta_k < \frac{\pi}{p} \quad k = 1, 2, ..., p \quad \text{eq 3.8}$$

The pulse width varies as the sine of the position angle $\alpha_k$ (angle at the center of the pulse) in the half period $T_0/2$:

$$\delta_k = \delta_{k, \text{max}} \sin \alpha_k \quad \text{eq 3.9}$$

The maximum pulse width occurs at the angles $\pi/2$ and $3\pi/2$ and is given by:

$$\delta_{k, \text{max}} = a \frac{\pi}{p} \quad a \leq 1 \quad \text{eq 3.10}$$

Parameter $a$ is called the PWM constant (modulation index) and is defined as the ratio of the amplitude of the sinusoidal modulating signal and the amplitude of the triangular carrier.

Amplitude of the $n^{th}$ harmonic of the inverter output voltage waveform is:
\[ V_{\text{om}} = \sum_{k=1}^{p} \frac{4V_s}{n\pi} \sin n\alpha_k \sin \frac{n\delta_k}{2} \] ..............................eq 3.11

Based on the above derivation of the Inverter Model, figure 3.14 illustrates the inputs, constants and outputs from the Inverter Model

![Inverter Model Diagram]

**Figure 3.14: Inverter Model**

The *m-file* of the Inverter Model is documented in Appendix B. Figure 3.15 shows the output from a simulation using the Inverter Model. The model was connected to the MSX60 model and MPPT model under the following conditions:

- \( G = 1000 \, \text{W/m}^2 \)
- \( T = 25 \, ^\circ\text{C} \)
- \( f_0 = 50 \, \text{Hz} \)
- \( p = 15 \)
3.5.2 Power Flow Model

A common way of arranging the switches in a power inverter is the full-bridge, also called the H-bridge as shown on the next page. In this arrangement, both positive and negative voltages and currents can be applied to the load. The bridge can either be a Voltage Source Inverter (VSI) or a Current Source Inverter (CSI). In a VSI, the DC-link is voltage stiff, capacitive, and the load is current stiff, inductive. In a CSI it is the opposite. When the inverter is connected to the grid and a high quality of grid current is desired the VSI must be used. The CSI gives a square wave shaped grid current.
The H-bridge in the figure above is connected to the grid and can apply \( +U_{dc} \) (Sw1 and Sw4 on), \( -U_{dc} \) (Sw2 and Sw3 on) or zero voltage (Sw1 and Sw3 on or Sw2 and Sw4 on) on the output, \( u_{out} \). To force current into the AC-bus, \( U_{dc} \) must be higher than the peak value of the bus voltage to be able to create a sinusoidal current.

From the simplified scheme of the inverter in figure 3.17 a phasor diagram can be constructed. \( U_{PWM} \) will generate a sinusoidal current to the grid, provided the grid voltage, \( U_g \) is sinusoidal and the components are linear. The phasors below are the fundamental components of the voltages and currents. They rotate counter-clockwise at 50 Hz.
The phase shift, \( \phi \), represents the difference in phase for the grid current and the grid voltage. A positive \( \phi \), will make the inverter ‘consume’ reactive power while a negative \( \phi \), as in the figure above will provide reactive power to the grid. For a PV-Inverter, \( \phi \), is normally set to zero so only active power is produced at a minimum of loss. From the figure the following equations can be derived:

\[
U_{PWM} = \sqrt{U_{PWM,X}^2 + U_{PWM,Y}^2} \quad \text{eq 3.12}
\]

\[
\alpha = \arctan \frac{U_{PWM,Y}}{U_{PWM,X}} \quad \text{eq 3.13}
\]

Where:

\[
U_{PWM,Y} = -U_R \sin \phi + U_L \cos \phi = -I_g R \sin \phi + I_g \omega L \cos \phi \quad \text{and}
\]

\[
U_{PWM,X} = U_g + I_g \cos \phi + U_L \cos \phi = U_g + I_g R \cos \phi + I_g \omega L \sin \phi \quad \text{eq 3.14}
\]

If we set the phase shift to zero:

\[
U_{PWM} = \sqrt{U_g^2 + I_g^2 \omega^2 L^2} \quad \text{Assuming that } R \text{ is very small} \quad \text{eq 3.15}
\]

Figure 3.19 shows the time diagram if we synchronize the grid current with the grid voltage:
Figure 3.19: Phasor Diagram with grid current and voltage in phase

\[ I_g = \frac{U_L}{\omega L} \] .................................eq 3.17

\[ P_g = I_g U_g \] ....................................................eq 3.18

Simplifying the Power Equation:

\[ P_g = \frac{U_g U_L}{\omega L} \]

but \( X_L = \omega L \) and \( U_L = U_{PWM} \sin \alpha \)

Therefore:

\[ P_g = \frac{U_g U_{PWM}}{X_L} \sin \alpha \] ......................eq 3.19

From equation 3.19. It is seen that \( U_{PWM} \) and \( \alpha \) can be control parameters in the Power flow model. \( U_{PWM} \) can be varied by varying the modulation index of the PWM inverter.

The modulation index is the PWM constant given as \( a \) in equation 3.10. More complex forms of Sine-PWM use a non-sinusoidal variation of pulse width aiming to
increase $U_{pwm}$. In this project the modulation index and load angle is used to control the power transfer from the PV system to the grid.

### 3.5.3 Modeling Power loss in an Inverter

MOSFETs have completely taken over low-voltage, medium-power high-frequency switching applications. In this project MOSFETs were selected for the purposes of modeling switching functions in an inverter. In the next phase of the research, hardware realisation used the IRFP064N MOSFETs.

Figure 3.20 below shows the switching waveform in a MOSFET based inverter.

![Switching waveform of MOSFETS](image)

**Figure 3.20**: Switching waveform of MOSFETS
The power loss is calculated from:

\[ P_{\text{loss}} = P_{\text{sw\_on}} + P_{\text{on}} + P_{\text{sw\_off}} \] \quad \text{eq 3.20}

where

\[ V_F = I_o r_{DSon} \] \quad \text{eq 3.21}

\[ P_{\text{sw\_on}} = \frac{1}{2} \left[ V_{DD} \frac{I_o (t_2 - t_1)}{2} + I_o \frac{(V_{DD} - V_F) t_f}{2} + V_F t_f \right] \] \quad \text{eq 3.22}

\[ P_{\text{on}} = V_F I_o \] \quad \text{eq 3.23}

\[ P_{\text{sw\_off}} = \frac{1}{2} \left[ I_o \frac{(V_{DD} - V_F) t_f}{2} + V_F t_f \right] + V_{DD} \frac{(t_3 - t_2) I_o}{2} \] \quad \text{eq 3.24}

from:

\[ t_2 - t_1 = R_g (C_{gs} + C_{gd}) \ln \left( \frac{g_m V_{DD}}{g_m (V_{DD} - V_T) - I_o} \right) \] \quad \text{eq 3.25}

\[ t_3 - t_2 = \frac{(V_{DD} - V_F) C_{gd}}{I_g} \] \quad \text{eq 3.26}

Where \( I_g = \frac{V_{DD} - (V_T + I_o)}{g_m R_g} \) \quad \text{eq 3.27}

The on-state resistance of power MOSFETs increases with temperature:

\[ r_{DSon}(T) = r_{DSon}(25^\circ C) \left( \frac{T}{300} \right)^{2.3} \] \quad \text{eq 3.28}

where \( T \) is in degrees Kelvin.

Transconductance of MOSFETs has a negative temperature coefficient:

\[ g_m(T) = g_m(25^\circ C) \left( \frac{T}{300} \right)^{-2.3} \] \quad \text{eq 3.29}
The threshold voltage $V_T$ also has a negative temperature coefficient, typically $-6mV/°C$ \[\text{[B1]}\]

Appendix B contains the m-file for the Power loss model of an Inverter.

3.5.4 Inverter Model using SimPower Systems Blocks
SimPowerSystems is a modern design tool that allows scientists and engineers to rapidly and easily build models that simulate power systems. SimPowerSystems uses the Simulink environment, allowing you to build a model using simple click and drag procedures. Not only can you draw the circuit topology rapidly, but your analysis of the circuit can include its interactions with mechanical, thermal, control, and other disciplines. See Figure 3.21 and 3.22 for the model and its parameters

![Figure 3.21: Inverter Model Using SimPower Systems](image)

![Figure 3.22: Parameters for the Inverter Model](image)
3.6 Complete Model and Simulation System

Two approaches to the development of the complete Model and Simulation System were looked at:

1.) Using Matlab Language

Appendix B documents a complete simulation code of single phase grid connected PV system. The following is an output from the Simulation of a single phase grid connected PV system using Parameters at STC:

-------------Captured from Matlab Workspace-----------------------------
Simulation Program for Grid connected PWM inverter with PV as a DC source

By Emanuel Rashayi
Ver 1.1, 10/03/2006

Enter minimum Voltage for MPPT Algorithm:0
Enter the increment value for MPPT Algorithm:0.1
Enter the Maximum Voltage for MPPT algorithm:30
Enter the solar Irradiation :1000
the switching frequency of the inverter(Hz)= 2500
the frequency of the output fundamental voltage(Hz)= 50
the initial modulation index of the PWM inverter(0<ma<1)=0.8
The rms voltage of the AC bus(50Hz) = 12
The number of MXS60 modules in parallel = 1
The number of MXS60 modules in series = 2
The inductor size of the inverter in mH : 3.8
startpulse (in radians) endpulse (in radians) pulsewidth

0.0597 0.0660 0.0063
0.1791 0.1979 0.0188
0.2986 0.3297 0.0311
0.4184 0.4612 0.0428
0.5386 0.5924 0.0539
0.6591 0.7232 0.0641
0.7802 0.8535 0.0733
0.9018 0.9831 0.0813
1.0241 1.1122 0.0881
1.1471 1.2405 0.0935
1.2708 1.3682 0.0974
1.3953 1.4950 0.0997
1.5205 1.6211 0.1005
1.6466 1.7463 0.0997
<table>
<thead>
<tr>
<th>Startpulse (in radians)</th>
<th>Endpulse (in radians)</th>
<th>Pulsewidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.7734</td>
<td>1.8708</td>
<td>0.0974</td>
</tr>
<tr>
<td>1.9011</td>
<td>1.9945</td>
<td>0.0935</td>
</tr>
<tr>
<td>2.0294</td>
<td>2.1175</td>
<td>0.0881</td>
</tr>
<tr>
<td>2.1584</td>
<td>2.2398</td>
<td>0.0813</td>
</tr>
<tr>
<td>2.2881</td>
<td>2.3614</td>
<td>0.0733</td>
</tr>
<tr>
<td>2.4184</td>
<td>2.4825</td>
<td>0.0641</td>
</tr>
<tr>
<td>2.5492</td>
<td>2.6030</td>
<td>0.0539</td>
</tr>
<tr>
<td>2.6804</td>
<td>2.7232</td>
<td>0.0428</td>
</tr>
<tr>
<td>2.8119</td>
<td>2.8430</td>
<td>0.0311</td>
</tr>
<tr>
<td>2.9437</td>
<td>2.9625</td>
<td>0.0188</td>
</tr>
<tr>
<td>3.0756</td>
<td>3.0819</td>
<td>0.0063</td>
</tr>
</tbody>
</table>

The rms Value of the output voltage fundamental component =

\[ v_{1\text{rms}} = 18.4916 \]

The rms Value of the output Voltage =

\[ v_{\text{rms}} = 23.9290 \]

The rms value of the load current =

\[ I_{\text{rms}} = 5.0798 \]

The average value of the supply current to the inverter is

\[ I_{\text{av}} = 2.6393 \]

The RMS value of the supply current to the inverter is =

\[ I_{\text{rms}} = 3.9720 \]

The load angle of the inverter in degrees =

\[ \phi = 18.9861 \]

the voltage and maximum power point

\[ V_{\text{mpp}} = 34 \]

The maximum power point of the solar module

\[ P_{\text{in}} = 120.9447 \]
Performance parameters are
THDvo =
  82.1321
THDIo =
  4.9828
Elapsed time is 3.976000 seconds.

Figure 3.23: Simulation Results at STC

2.) Using Simulink Blocks

The simulation system using Simulink Blocks is divided into two parts;

i.) PV Simulation system

ii.) Inverter and Load Simulation system

Figure 3.24 overleaf shows the PV Simulation system in Simulink. Other Power and Voltage values can be observed by varying the environmental conditions (i.e. solar
irradiance and temperature). Figure 3.25 shows the blocks for the inverter and load Simulation system. Figure 3.26-3.28 captures the outputs from the simulation system.

**Figure 3.24:** PV simulation System

**Figure 3.25:** Inverter and Load Simulation system
Figure 3.26: Simulation Scope Output

Figure 3.27: Harmonic Analysis (output Voltage) using Powergui
3.6.1 Discussion of Simulation Results

In this design of the simulation models, the 12 V ac bus was chosen as this will be used in the actual realization of a prototype. Generally 12/220 V transformer is considered standard transformer. The simulations gives an indicator for a given system the extent of the Total harmonic distortions for current and voltage. This gives the degree of power quality of the system. The efficiency of the system given does not include the PV panel as the simulations concentrated on the grid connected inverter system.

It can be observed that the rms load current and rms supply current are different as a result of the different voltage levels between the input to the inverter and the output. The
inductor in the output circuit smoothens the output current resulting in lower THD than
the supply current.

As the output voltage is Pulse width modulated, there are a substantial amount of
harmonic components as seen by a high THD (>70%). This gives rise to a lower
fundamental voltage than the output voltage by ….

From the two scenarios of the simulations: one from MATLAB and another from
Simulink. The results using an example of THD for current shows a variance of 16.9%.
The difference in the THD can be attributed to the fact that the Simulink model uses
Physical modeling which uses the properties of actual components as opposed to
theoretical analysis done in MATLAB. Hence Simulink can be preferred.

These simulations will be validated through development of a prototype of the system.
Chapter 4

Design of a Hardware Prototype

4.0 Introduction

This chapter reports on the design and realization of a PV inverter for a single phase grid connected system. Specifications are given for this particular system. The major objective is to design and realise a PV inverter which can be used to carry out measurements to support the results of the simulations in the previous chapter. The inverter uses an inexpensive Siemens 80C535 microcontroller, which uses a PWM technique. Emphasis is on power transfer and high power quality.

4.1 Design of the PV inverter

The PV inverter has the following specifications:

1.) The voltage from the PV module (MSX60) is 15-25 V
2.) Rating of 120VA
3.) AC bus voltage of 12 V (rms)

The design phase involves the selection of the switches used in the design of the Full Bridge inverter, design of the inductor for the filtering function and the hardware for the control system.

4.1.1 Main Circuit

Figure 4.1 shows the main circuit. The inverter uses a Full-bridge (H-bridge) configuration. The H-bridge consists of four MOSFET-transistors. A capacitor, C, makes the voltage stiff and an inductor, L, filters the output current to the low voltage AC-bus.
An H-bridge can apply $+U_{dc}$ (Sw1 and Sw4 on), $-U_{dc}$ (Sw2 and Sw3 on) or zero voltage (Sw1 and Sw3 on or Sw2 and Sw4 on) at the output, $u_{out}$. To force current into the AC-bus, the dc voltage, $U_{dc}$, must be higher than the top value of the bus voltage in order to create a sinusoidal current.

The choice of switches is naturally the MOSFETs for low power and low voltage applications. The MOSFETs were selected for the following reasons:

- Easy gate drive circuit
- Higher speed of operation
- Better safe operating area
- Low conducting losses, though higher than IGBTs, e.g. $R_{D_{son}}$ of $8\,m\Omega$ available for 55 V, 100A.

- Additionally, they have parasitic, anti-parallel diodes that can be used as freewheel-diodes. If these diodes show poor performance (long reverse recovery time or high forward conducting voltage) external diodes, preferably Schottky diodes should be used in parallel.
The selected MOSFETs: IRFP064N, have been tested without Schottky diodes. The capacitance on the DC-link supplies the H-bridge with a stiff voltage. Dimensioning is such that the 100 Hz ripple on the voltage is kept within reasonable values. A capacitance of 2200 µF gives a worst-case ripple of 3% [29]. The capacitor must also be able to carry a fairly high current; roughly 1.5-2 times the mean dc current. A capacitor with a low equivalent series resistance should be employed, due to the filtering function and to minimize the heat-up of the capacitor in order to avoid shortening its lifetime.

An analysis of current and voltage for the DC capacitor was done, this is shown in Appendix C.6. The model was simulated in MATLAB and effects of using different values of capacitance were observed. A capacitance of 2200uF was chosen as it gives a 100 Hz ripple of 3.7%. Figure below shows the ripple captured in MATLAB using values obtained in simulations in the previous chapter.

![Figure 4.2: DC Capacitor Voltage Ripple](image)

**Figure 4.2:** DC Capacitor Voltage Ripple
The design of the inductors, $L$, is important, considering both power quality and efficiency. The core material together with the variation in flux density determines the iron losses (eddy currents and hysteresis). If the switching frequency is increased, the ripple losses will normally decrease (not for the fundamental frequency though), but then the switching losses in the transistors will increase. A high inductance will also reduce the ripple current and, therefore, decrease the ripple losses but, on the other hand, will increase the weight and cost of the inductance.

The design of the inductor involved selection of a suitable core from Micrometals. The constraints in this regard were availability of the cores in the region and the cost of the core. Iron powder toroidal cores were selected. Software from Micrometals was used to come up with T400-26 core. Two cores were used to give an inductance greater than 3$mH$ so as to achieve the intended power quality. The inductance of between 3 and 4 $mH$ was selected based on the simulations in the previous chapter. The following figures give details on the design.

![Figure 4.3: Power Line Frequency Inductor Analysis](image-url)
Figure 4.4: Inductance Vs Current

With the inductor chosen, should the current in the circuit be lower than the nominal, the value of the inductance decreases, as shown on the figure above, this will result in high THD of current. Power quality decreases if power lower than nominal is injected into the grid.

4.1.2 Control Circuit

The block diagram of the main circuit and the controller is shown in figure 4.5

The Siemens 80C535 microcontroller has the overall responsibility of all control functions. The specific roles of the microcontroller are as follows:

(i) produces PWM signals for the IR2113 driver circuit

(ii) Controls the output voltage of the PWM inverter by varying the modulation index. This is implemented as a Maximum power point algorithm in the microcontroller.
(iii) Receives zero crossing pulses, which are phase shifted by a defined load angle, and derived from grid voltage and performs synchronization with PWM output voltage.

(iv) Checks AC voltage and frequency for any deviations. If AC voltage increases/decreases or switched OFF, the microcontroller will send stop commands to isolate the inverter circuit. Frequency is also monitored and any deviations by +/-0.5% will result in the inverter being isolated from the grid.

**Figure 4.5**: Block diagram of the Main circuit and controller
(v) Checks the DC voltage for any decrease below the grid voltage. Always this voltage should be higher than the grid voltage.

These roles were fully realized as it will be shown in the next chapter on software development.

4.1.3 Power MOSFET Drive Circuits

The transistor drive circuit was designed using the IR2113 power MOSFET driver. The IR2113 is a high voltage, high speed power MOSFET driver with independent high and low side reference output channels. Logic inputs are compatible with standard CMOS or TTL output. The floating channel can be used to drive an N-channel power MOSFET in the high side configuration which operates up to 500 or 600 Volts. Figure 4.6 shows the implementation of the Power MOSFET driver circuit using the IR2113 drivers [30].

![Figure 4.6: Implementation of the IR2113 Power MOSFET driver circuit](image)

The IR2113 can operate on the bootstrap principle or with a floating power supply. With a floating power supply the cost impact of isolated supply is significant as each high side MOSFET requires a floating power supply. Bootstrap mode is simple and inexpensive though with limitations.
The shut down pin (SD) of the IR2113 is used to shut down the inverter for control purposes. A Logic 1 will shut down the inverter.

In order to drive the Power MOSFETs. The following condition should be fulfilled:

1. \[ V_{gs} > V_{th} \]

The threshold voltage of the IRFP604PN is 2 and 3 V. The MOSFETS were driven with 15 V in this project.

4.1.4 Voltage sensing Circuits

Measurements of Voltage signals used AD622 instrumentation amplifiers. The AD622 is a low cost, moderately accurate instrumentation amplifier that requires only one external resistor to set any gain between 2 and 1,000. It also provides performance and space improvements.

![Instrumentation Amplifier](image)

**Figure 4.7:** Instrumentation Amplifier

4.1.5 Current Sensing Circuit (AC Current)

For AC current sensing, a PCB mountable voltage transducer, based on the Hall Effect was used. The unit (LV 25-P) provides galvanic isolation between primary and secondary circuits. A current which flows through an external resistor, about 100 Ω, in series with the secondary circuit of the unit will result in a voltage across the external resistor. This voltage will be proportional to the current flowing in the primary circuit (see figure 4.8).
4.1.6 Low Voltage 12 AC bus

The 12 V AC bus is provided by a 225 / 12 V, 120VA single phase transformer. Figure 4.9, 4.10 and 4.11 shows the characteristics of the AC bus.

Figure 4.9: Voltage Waveform of the AC bus
Figure 4.10: Total harmonic Distortion of Voltage on the AC bus

Figure 4.11: Harmonic components of voltage on the AC bus
With the transformer used, there is a total harmonic distortion of 3.6% and the dominant harmonics are the $3^{rd}$, $5^{th}$, $7^{th}$ and $9^{th}$. These harmonics if high can impact negatively on the voltage level of the fundamental component.

### 4.1.7 Relay Circuit

Figure 4.8 shows the relay circuit for isolating the PWM inverter from the Grid interconnection if any of the following conditions occurs:

1. Frequency drift from 50 Hz by more than 0.5 %
2. Voltage from the PWM output becomes lower than the voltage from the AC bus (12V)
3. Islanding condition

![Relay Circuit Diagram](Figure 4.12: Relay Circuit)

### 4.1.8 SAB80C535 Microcontroller

The Siemens 80C535 microcontroller provides the entire control functions. The figure 4.13 overleaf shows the pin layout. See Appendix C.3 for details.
The features which are mainly used in this research project are:

4. 16-bit reload, compare, capture capability
5. A/D converter, 8 multiplexed analog inputs, programmable reference voltages
6. Full-duplex serial port, 4 modes of operation, fixed or variable baud rates
7. Three 16-bit timer/counters
8. Six 8-bit parallel I/O ports

**4.1.9 A Grid Synchronization Technique**

Optimization of power transfer from the PV system to the Grid requires that the current injected into the grid should always be in phase with the grid voltage. This allows operation at unity power factor and injection of power at minimum loss.
In order for the current to be in phase with the grid voltage, a grid synchronization technique was implemented.

As shown in figure 4.14, if we increase the load angle of $U_{pwm}$ and $U_g$ from $\delta_1$ to $\delta_2$, the phase angle changes from $\phi_1$ to $\phi_2$. The idea is that there is a load angle between $U_{pwm}$ and $U_g$, where $U_g$ will be in phase with $I_g$. This is the maximum power point of the interface between the PV and grid interconnection.

![Figure 4.14: Phasor Analysis](image)

Figure 4.15 shows a typical instant of load angle and shows a small phase angle between the Grid current and the grid voltage, for maximum power transfer the phase angle should be zero.
The actual implementation involves shifting the sensed grid voltage using the RC circuit with a variable resistor shown in Figure 4.16. The sensed grid voltage is shifted by an angle which is equal to the load angle determined from simulations in the previous chapters.

\[ C = 1.2 \mu F \]

The load angle can be varied by changing the resistance of the circuit. From the above circuit, \( v_{out} \) leads \( v_{in} \) by an angle equal to \( 2\pi fRC \) which is the load angle between the Inverter voltage and grid voltage.
The output of the RC circuit is supposed to be in phase with the output from the PWM inverter. This will effectively make the PWM signal ahead of the grid voltage by a load angle of $2\pi fRC$. To realize it the zero crossing detector circuit shown in figure 4.17 is used. The LM311 is a voltage comparator and will produce pulses with amplitude of 15V starting at zero crossing of the impressed sinusoidal voltage. This is reduced to 5 V in the output stage using a 4N25 opto-isolator. The opto-isolator is also used to provide isolation between input stage and the output stage as the output signal is fed into the SAB80C535 microcontroller. The rising edge of the output pulses will coincide with the start of PWM pulses and will end at the falling edge and the process starts all over again. This is looked at in detail in the next chapter.

**Figure 4.17: Zero Crossing detection**

The next chapter looks at the development of system software based on the hardware discussed in this chapter.
Chapter 5

Development of System Software

5.0 Introduction

The hardware described in the preceding chapter will only work if the SAB80C535 microcomputer board is programmed. This chapter describes the various software routines which were developed and tested. In order to shorten the software development cycle, a High Level Language: BASIC was used in this project. The environment used was BASCOM-8051 IDE. This environment allows the programmer to seamlessly switch between a High level Language: BASIC and a Low Level Language: Assembly Language so as to optimize code development.

The software development is broken down into the following software modules:

1. Sinusoidal PWM generation
2. Maximum Power Point Tracking
3. Grid Synchronization Technique
4. Grid Voltage/ frequency Checking
5. Input Voltage (Udc) monitoring
6. Calculation of Power injected into the Grid
7. Isolation of the Inverter

5.1 Sinusoidal PWM generation

The PWM signals are generated on P1.1 and P1.2 of the SAB80C535 microcomputer board. It uses the Output Compare Function.
5.1.1 Compare Function

The 16-bit value stored in a compare register is compared with the contents of the timer 2 register. If the count value in the timer 2 register matches the stored value, an appropriate output signal is generated at a corresponding port pin and an interrupt is requested. The contents of the compare register are varied sinusoidally, producing PWM signals at the port pin.

Compare mode 0 was chosen. Upon matching the timer 2 and compare register contents, the output signals changes from low to high: it will then go back to low upon timer 2 overflow. As long as compare mode 0 is enabled, the appropriate output pin is controlled by the timer circuit only, and not the user.

5.1.2 Compare Interrupt

When using the port lines as compare outputs, the input line from the port pin to the interrupt system is disconnected. The interrupt input will be directly connected to the compare signal thus providing a compare interrupt.

The compare interrupt is used to change the contents of the compare register so as to determine the level of the port outputs for the next “compare match”. When an interrupt request flag is set the interrupt service routine is called. This service routine then sets up all the necessary parameters for the next compare event.

5.1.3 Look-up Tables for PWM generation

Two tables are created using Excel spreadsheet. One is for the CRC register and another for the CC1 and CC2 registers. Calculation of the table values is based on the sine PWM inverter model described in chapter 3. The table below is an extract from the spreadsheet calculation.
Table 5.1: CRC and CCx values

<table>
<thead>
<tr>
<th>No.</th>
<th>Pulse</th>
<th>Reload Value (CRC)</th>
<th>Compare(CCx)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>66257</td>
<td>65492</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>64980</td>
<td>65408</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>64983</td>
<td>65330</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>64967</td>
<td>65260</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>64993</td>
<td>65203</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>66001</td>
<td>65160</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>66009</td>
<td>65134</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>66018</td>
<td>65125</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>66027</td>
<td>65134</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>66035</td>
<td>65160</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>66044</td>
<td>65203</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>66051</td>
<td>65260</td>
<td></td>
</tr>
</tbody>
</table>

5.1.4 Flowchart for Initialisation Routine and Interrupt Handler

![Flowchart](image)

**Figure 5.1: Initialization Routine**
Figure 5.2: Interrupt Handler for int4 & int5 interrupts
5.2 Maximum Power Point Tracking

The maximum power point tracking strategy employs the ‘perturb and observe’ method using a convergence technique [18].

In order to extract maximum power from the PV, the maximum power point tracker ideally should stay always at the maximum power point. The convergence technique uses three 8-bit registers which stores indices which point to different tables in memory with different modulation indices, the lower the modulation index, the lower the voltage output of the inverter.

At the start, D0 is initialized to a value of 9 and D1 to a value of 1. The average of D0 and D1 is calculated and stored in D2. The grid voltage and current are measured and power, P0 is calculated. The value of D2 is then decremented and again voltage and current measured. Power, P1 is calculated. P1 and P0 are compared; if they are equal the tracker will stay at that power point for a defined time. If P0 is greater than P1 the value of D2 is stored in D1, else it will be stored in D0. The process is repeated until the maximum power point is reached.

Figure 5.3: Interrupt Handler for Timer 2 Interrupt
5.2.1 Flowchart for Maximum Power Point Tracking

![Flowchart for Maximum Power Point Tracking]

5.3 Grid synchronization

By checking the zero crossing of the shifted grid signal a pulse train can be created which will be at the same frequency as the grid voltage. This pulse train is used as the reference for the operation of the inverter. The rising edge of the pulse will start the positive PWM pulses of the inverter and the falling edge will start the negative PWM pulses of the
inverter. This will ensure the inverter locks to the pulse train which will basically be the same as locking to the phase shifted grid signal. This approach gives a very stable Inverter-Grid interaction.

5.4 Grid Voltage and Frequency checking & Islanding Condition

The control system of the inverter system should constantly check for frequency and voltage variations from the normal. If the frequency and voltage increases or decreases beyond the set limit, the control system should isolate the inverter from the grid network. The inverter checks every 100 cycles (providing a large window size for shutting down the inverter) for grid failure and switches off if grid voltage disappears. During the checking of the grid voltage, the MOSFET drivers are shut down temporarily using the shutdown pins.

Appendix E documents the complete program integrating all the software routines discussed in this chapter.
Prototype: Experimentation & Results

6.0 Introduction

This chapter captures results of experimentation with the prototype which was developed. Various outputs of voltage and current were captured using the NI USB-6009 Data Acquisition System. Analysis of the signal is done using Labview Student Edition. The virtual instrument developed in Labview displays the THD of the signal captured by the Data Acquisition System (see Appendix E.4).

The approach which was taken looked at characteristics of the inverter before it was connected to the grid. The output waveforms were captured for various switching frequencies and also the driver signals to observe basic inverter functionality. The next step looked at the characteristics of the inverter when it was connected to the grid. The current waveform was captured and its characteristics observed. This also involved demonstration of power transfer to the grid by capturing the grid voltage and PWM output voltage. A leading load angle of PWM output voltage demonstrated power transfer. The system because of its small size will not alter the grid voltage.

6.1 Standalone Inverter Characteristics

Before one can connect an inverter to the grid there is need to look at the characteristics in standalone mode. In this particular mode grid synchronization is disabled. This mode gives an ‘ideal behaviour’ of the inverter and various output waveforms at various switching frequencies are investigated and also the driver signal waveforms.
Figure 6.1 shows the output waveform of the Inverter at a switching frequency of 1.5 kHz ($p = 15$ pulses per half period). The H-Bridge was driven by signals shown in figure 6.2.

**Figure 6.1:** PWM Output voltage waveform at $p = 15$ pulses

**Figure 6.2:** Power Mosfet Driver Signals, $p = 15$
Figure 6.3 – 6.5 shows the output voltage waveforms at various switching frequencies.

**Figure 6.3**: Voltage Output of Sinusoidal PWM inverter, \( p = 5 \) pulses

**Figure 6.4**: Voltage Output of Sinusoidal PWM inverter, \( p = 7 \) pulses
Figure 6.5: Voltage Output of Sinusoidal PWM inverter, p = 9 pulses

The microcontroller could produce pulse per half period up to 25 pulses. Above 25 pulses, the output pins started oscillating. The inverter circuit could respond positively with the output waveforms shown above for various switching frequencies. This demonstrated the functionality of the inverter before connecting to the grid. The variation of the pulse width as shown by equation 3.9 in chapter 3 is evident if one looks at figure 6.3, 6.4, and 6.5. As the switching frequency is increased from 1.5 kHz, the performance of the freewheel-diodes can be observed. The MOSFETs used have internal free-wheeling diodes. The characteristics of the waveforms at high switching frequencies depend on the properties of the MOSFETs used in terms of their switching characteristics. Appendix shows the characteristics of the IRFP064N.

6.2 Power Transfer

The diagram below shows the block diagram of the setup which was used to demonstrate power transfer.
Initially when the inverter is offline (which means shut down) the grid supplies power to the load (a light bulb) at unity power factor. The Power from the DC source was adjusted by changing the current limit of the source, the voltage from the grid side was adjusted using an auto transformer. This was done as the DC source voltage decreases appreciably when connected to the grid as the grid is an infinite load.

**Figure 6.6:** Demonstration of Power Transfer

<table>
<thead>
<tr>
<th>Power from DC source (W)</th>
<th>$P_{inv}$ (W)</th>
<th>Power factor(Inverter)</th>
<th>$P_{load}$ (W)</th>
<th>$P_{grid}$ (W)</th>
<th>Power Factor (grid)</th>
</tr>
</thead>
<tbody>
<tr>
<td>40</td>
<td>36</td>
<td>≈ 1</td>
<td>60</td>
<td>24</td>
<td>&gt;0.9</td>
</tr>
<tr>
<td>60</td>
<td>53</td>
<td>≈ 1</td>
<td>60</td>
<td>7</td>
<td>&gt;0.9</td>
</tr>
<tr>
<td>75</td>
<td>64</td>
<td>≈ 1</td>
<td>60</td>
<td>4</td>
<td>&gt;0.9</td>
</tr>
<tr>
<td>80</td>
<td>64</td>
<td>≈ 1</td>
<td>60</td>
<td>4</td>
<td>&gt;0.9</td>
</tr>
<tr>
<td>100</td>
<td>80</td>
<td>≈ 1</td>
<td>60</td>
<td>20</td>
<td>&gt;0.9</td>
</tr>
<tr>
<td>120</td>
<td>94</td>
<td>≈ 1</td>
<td>60</td>
<td>34</td>
<td>&gt;0.9</td>
</tr>
</tbody>
</table>

**Table 6.1:** Power Transfer Results
Table 6.1 shows power transfer to the grid at power factor greater than 0.9 at power levels above that of the power rating of the bulb.

Figure 6.7 shows the waveforms for grid voltage and Inverter voltage leading.

![Image of grid and inverter voltage waveforms]

**Figure 6.7:** Grid and Inverter Voltage waveforms

In order for power to be transferred to the grid, the Inverter voltage should at least lead the grid voltage by a load angle obtained in equation 3.19 in chapter 3, distortions on the inverter voltage is due to the harmonic components in the waveform.

### 6.3 Grid Current waveform

As the number of pulses per half period is increased the inductance size required to smoothen the output current decreases. The limitation on increasing the switching frequency of the inverter is on the microcontroller’s machine cycle. In this project the crystal frequency used was 12 MHz, giving a machine cycle of 1 µS. Increasing the
switching frequency beyond 2.5 kHz started giving problems of oscillations at the PWM output pins on the microcontroller.

Figure 6.8 shows the captured current signal using a Data Acquisition System

![Current Output from Sinusoidal PWM inverter, p = 25 pulses](image)

**Figure 6.8**: Current Output from Sinusoidal PWM inverter, p = 25 pulses

Selection of inductor size was based on the simulation results in chapter 3. The simulation results recommended at least 3 mH for the prototype.

### 6.4 Fourier Analysis of Grid Current

To determine the dominant harmonics in the current signal, Fourier analysis was employed. Figure 6.9 shows the frequency components of the current signal at p = 25 pulses per half period. The dominant harmonics observed are the 3rd, 5th, 7th and 9th harmonics. These are normal harmonics expected with this kind of inverter [29]
Figure 6.9: Frequency Spectrum of Current Waveform, p = 25 pulses

6.5 Total Harmonic Distortion

When tens or hundreds of inverters are connected to the grid it is very important to have output currents of good quality. If not, problems might occur on the grid, or in equipment connected to it. Figure 6.10 shows the Total Harmonic Distortion measurements for the current signals at $p = 25$ pulses.
6.6 Discussion of Results

The developed prototype can successfully transfer power from the DC source to the utility grid. There is room to lower the THD of the current by increasing the inductor size of the inverter, however this will be at the expense of high core and copper losses of the inductor. Increasing the number of turns will increase the inductance. Careful selection of the core of the inductor can reduce the core losses appreciably; however this has to match cores available on the market. The efficiency of this inverter is seen to decrease as the inverter approaches full load (from 85% to about 80%). This agrees with research which has been done elsewhere [29].

In order to compare the results of the simulation with those obtained with the prototype, a simulation run for the parameters used in the prototype (current, voltage, inductor value at a particular current) was done.
Simulation Program for Grid connected PWM inverter with PV as a DC source

By Emanuel Rashayi
Ver 1.1, 10/03/2006

Enter minimum Voltage for MPPT Algorithm: 0
Enter the increment value for MPPT Algorithm: 0.1
Enter the Maximum Voltage for MPPT algorithm: 30
Enter the solar Irradiation: 645
Enter the Ambient temperature in degC: 25
the switching frequency of the inverter (Hz) = 2500
the frequency of the output fundamental voltage (Hz) = 50
the initial modulation index of the PWM inverter (0<ma<1) = 0.8
The rms voltage of the AC bus (50Hz) = 12
The number of MXS60 modules in parallel = 1
The number of MXS60 modules in series = 2
The inductor size of the inverter in mH: 2.1

startpulse (in radians) endpulse (in radians) pulsewidth
0.0597     0.0660     0.0063
0.1791     0.1979     0.0188
0.2986     0.3297     0.0311
0.4184     0.4612     0.0428
0.5386     0.5924     0.0539
0.6591     0.7232     0.0641
0.7802     0.8535     0.0733
0.9018     0.9831     0.0813
1.0241     1.1122     0.0881
1.1471     1.2405     0.0935
1.2708     1.3682     0.0974
1.3953     1.4950     0.0997
1.5205     1.6211     0.1005
1.6466     1.7463     0.0997
1.7734     1.8708     0.0974
1.9011     1.9945     0.0935
2.0294     2.1175     0.0881
2.1584     2.2398     0.0813
2.2881     2.3614     0.0733
2.4184     2.4825     0.0641
2.5492     2.6030     0.0539
2.6804     2.7232     0.0428
2.8119     2.8430     0.0311
2.9437     2.9625     0.0188
3.0756     3.0819     0.0063

The rms Value of the output voltage fundamental component =
v1rms =
  18.3828
The rms Value of the output Voltage =
vorms =
  23.7883
The rms value of the load current =
Iorms =
  3.2552
The average value of the supply current is
Isav =
  1.7436
The RMS value of the supply current is =
Isrms =
  2.5989
The load angle of the inverter in degrees =
phi =
  6.6474
the voltage and maximum power point
Vmpp =
  33.8000
The maximum power point of the solar module
Pin =
  77.4123
Performance parameters are
THDvo =
82.1321

THDIo =
12.9395

Elapsed time is 4.326000 seconds.

Figure 6.11: Simulation Results for Prototype Conditions

Within experimental limitations the simulations results correlates well the results obtained with the prototype. The simulation model developed can give a picture of the characteristics of the prototype before it is developed, this can make this model a design tool
Chapter 7

Conclusions and Future Work

This project looked at the modeling, simulation and optimization of single phase grid connected PV systems. A hardware prototype was developed based on the model which was created during the theoretical study. An Integrated inverter which uses a central transformer was selected as the best system configuration. Specific contributions to this particular research are as follows:

(a) A Cost effective inverter for grid connected PV systems

The inverter which was developed used inexpensive components and has the potential to compete with other inverters on the market. Most inverters on the market uses a DSP chip which is very expensive at the moment, the selection of the DSP chip is mainly to improve system performance at the expense of the cost of the system.

(b) PV model Block in Simulink

A contribution was made towards creation of a PV model block which can be used in the Simulink environment. This can be used in studies which needs a PV model Block. Currently Simulink does not have a model of a PV module. The model block which was developed correlates well with the PV modules from manufacturers.

(c) Design Tool for Single phase grid connected PV system

The simulation tool which was developed can be used as a design tool in designing single phase grid connected PV systems. The outcomes from this simulation tool correlates well with results from experimentation with the developed hardware.
(d) **A simple grid synchronization technique**

The grid synchronization involved a novel approach of shifting the grid voltage in advance and locking the PWM voltage to this particular voltage resulting in a leading PWM voltage. This technique ensures stability of operation and power transfer to the grid.

(e) **A Study tool for Harmonics produced by inverters for grid connected PV systems**

A contribution was made towards developing a tool for studying harmonics produced by inverters for grid connected PV systems. The good thing about this system is that of scalability. This can be adopted in developing countries like Zimbabwe, as capital requirements are more manageable.

As part of further work, there is need to connect the system with PV modules and carry out studies on the performance of the system on the ground. Something related to that is to formulate net-metering strategies which can benefit both the customer who owns this small power generator and the national power utility.

Another area which needs to be looked at is the effect on the electricity grid of connecting many small inverters. This is important for the Power Utilities to make a decision on the use of these inverters on their network.

As there is an anticipated Power shortage in the Southern African Power in 2007, the study carried out in this thesis can be applied as a Demand Side Management option. This can be used by residential customers in the low density areas who can afford it.
Bibliography


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References


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Appendix A

PV Modeling and Simulation

A.1 m-file of MSX60 PV model

```matlab
function Ia = msx60 (Va, Suns, TaC)

% constants used
k = 1.38e-23; % Boltzman's const
q = 1.60e-19; %charge on an electron

%Enter the following constants here, and the model will
%be calculated based on these for 1000W/m^2
A = 1.2;
Vg = 1.12;
Ns = 36;
T1 = 273 + 25;
Voc_T1 = 21.06/Ns;
Isc_T1 = 3.80;
T2 = 273 + 75;
Voc_T2 = 17.05/Ns;
Isc_T2 = 3.92;
TaK = 273 + TaC; % array working temp
TrK = 273 + 25; % reference temp
dVdI_Voc = -1.15/Ns/2; % dVdI at Voc per cell;

% when Va = 0, light generated current Iph_T1 = array short cct current
% constant 'a' can be determined from Isc vs T
Iph_T1 = Isc_T1*Suns;
a = (Isc_T2-Isc_T1)/Isc_T1*(1/(T2-T1));
Iph = Iph_T1*(1+a*(TaK-T1));
Vt_T1 = k*T1/q ;
Ir_T1 = Isc_T1/(exp(Voc_T1/(A*Vt_T1))-1);
Ir_T2 = Isc_T2/ (exp (Voc_T2/ (A*Vt_T1))-1); % not used
b = Vg*q/ (A*k);
Ir = Ir_T1*(TaK/T1)^(3/A)*exp(-b*(1/TaK-1/T1));
X2v = Ir_T1/(A*Vt_T1)*exp(Voc_T1/(A*Vt_T1));
Rs = -dVdI_Voc - 1/X2v; % series resistance per cell

% Ia = 0:0.01: Iph
Vt_Ta = A*k*TaK/q;

% Ial = Iph -Ir*(exp ((Vc+Ia*Rs)/ (Vt_Ta) - 1) ;
% solve for Ia: f (Ia) =Iph-Ia-Ir*(exp ((Vc+Ia*Rs)/Vt_Ta)-1) =0;
% Newton's method: Ia2 = Ia1 - f (Ia1)/f'(Ia1)
Vc = Va/Ns;
```

- 95 -
Ia = zeros (size (Vc));
% Iav = Ia;
for j = 1:5;
    Ia = Ia - (Iph-Ia-Ir*(exp ((Vc+Ia*Rs)/Vt_Ta)-1)) / (-I*(exp ((Vc+Ia*Rs)/Vt_Ta)-1)*Rs/Vt_Ta);
end

A.2 m-file for I-V characteristics of MSX60 PV model

% Script to show I-V characteristics of msx60 solar panel
% at 600, 800 and 1000 W/m^2 and 25 degC

Va = 0:0.5:24;
N = 0;
for V = 0:0.5:24;
    N = N + 1;
    Ia (1, N) = msx60 (V, 0.6, 25);
end
plot (Va, Ia, 'b');
axis ([0 24 0 4]);
xlabel ('Voltage (V)');
ylabel ('Current (A)');
Title ('MSX-60 I-V Characteristics');
hold on;
N = 0;
for V = 0:0.5:24;
    N = N + 1;
    Ia (1, N) = msx60 (V, 0.8, 25);
end
plot (Va, Ia, 'g');
N = 0;
for V = 0:0.5:24;
    N = N + 1;
    Ia (1, N) = msx60 (V, 1, 25);
end
plot (Va, Ia, 'r');

A.3 m-file for I-V characteristics of MSX60 PV model at different temperatures

% Script to show I-V characteristics of msx60 solar panel
% at 0, 25, 50 and 75 deg C

Va = 0:0.5:24;
N = 0;
for V = 0:0.5:24;
    N = N + 1;
    Ia (1, N) = msx60 (V, 1, 0);
end
plot (Va, Ia, 'b');
axis ([0 24 0 4]);
xlabel('Voltage(V)');
ylabel('Current (A)');
Title('MSX-60 I-V Characteristics');
hold on;
N=0;
for V = 0:0.5:24;
    N=N+1;
    Ia(1, N) = msx60(V, 1, 25);
end
plot(Va, Ia,'g');
N=0;
for V=0:0.5:24;
    N=N+1;
    Ia(1, N) = msx60(V, 1, 50);
end
plot(Va, Ia,'r');
N=0;
for V=0:0.5:24;
    N=N+1;
    Ia(1, N) = msx60(V, 1, 75);
end
plot(Va, Ia,'m');

A.4 m-file for P-V characteristics of MSX60 PV model under standard conditions.

% Script to show P-V characteristics of msx60 solar panel
% at 25 deg C

Va = 0:0.5:24;
N = 0;
for V = 0:0.5:24;
    N= N+1;
    Ia(1, N) = msx60(V, 1, 25);
    P (1, N) = Ia(1, N)*Va(1, N);
end
plot(Va, P,'b');
axis([0 24 0 80]);
xlabel('Voltage(V)');
ylabel('Power (W)');
Title('MSX-60 P-V Characteristics at G=1000W/m^2 and T=25 degC');

A.5 m-file for MSX-120 PV model

function Ia = msx120 (Va, Suns, TaC)

% constants used
k = 1.38e-23; % Boltzman's const
q = 1.60e-19; %charge on an electron

%Enter the following constants here, and the model will
%be calculated based on these for 1000W/m^2
A = 1.4;
Vg = 1.12;
Ns = 72;
T1 = 273 + 25;
Voc_T1 = 42.2/Ns;
Isc_T1 = 3.81;
T2 = 273 + 75;
Voc_T2 = 34.09/Ns;
Isc_T2 = 3.96;
TaK = 273 + TaC; % array working temp
TrK = 273 + 25; % reference temp
dVdI_Voc = -2.15/Ns/2; % dVdI at Voc per cell;

% when Va = 0, light generated current Iph_T1 = array short cct current
% constant 'a' can be determined from Isc vs T

Iph_T1 = Isc_T1*Suns;
a = (Isc_T2-Isc_T1)/Isc_T1*(1/(T2-T1));
Iph = Iph_T1*(1+a*(TaK-T1));
Vt_T1 = k*T1/q ;
Ir_T1 = Isc_T1/(exp(Voc_T1/(A*Vt_T1))-1);
Ir_T2 = Isc_T2/ (exp (Voc_T2/ (A*Vt_T1))-1); % not used
b = Vg*q/ (A*k);
Ir = Ir_T1*(TaK/T1)^(3/A)*exp(-b*(1/TaK-1/T1));
X2v = Ir_T1/(A*Vt_T1)*exp(Voc_T1/(A*Vt_T1));

Rs = -dVdI_Voc - 1/X2v; % series resistance per cell

% Ia = 0:0.01: Iph
Vt_Ta = A*k*TaK/q;

% Ia1 = Iph -Ir*(exp ((Vc+Ia*Rs)/ (Vt_Ta) - 1) ;
% solve for Ia: f (Ia) =Iph-Ia-Ir*(exp ((Vc+Ia*Rs)/Vt_Ta)-1) =0;
% Newton's method: Ia2 = Ia1 - f (Ia1)/f'(Ia1)
Vc = Va/Ns;
Ia = zeros (size (Vc));
% Iav = Ia;

for j = 1:5;
    Ia = Ia - (Iph-Ia-Ir*(exp ((Vc+Ia*Rs)/Vt_Ta)-1))/ (-1-(Ir*(exp ((Vc+Ia*Rs)/Vt_Ta)-1))*Rs/Vt_Ta);
end
A.6 MSX60 datasheets

**Safety Approved**
MSX60 and -64 modules are listed by Underwriters Laboratories for electrical and fire safety (Class C fire rating), certified by TUV Rheinland as Class II equipment, and approved by Factory Mutual Research for application in NEC Class 1, Division 2, Group C & D hazardous locations.

**Quality Certified**
These modules are manufactured in our ISO 9001-certified factories to demanding specifications, and comply with IEC 1215, IEEE 1292 and CEC 502 test requirements, including:
- repetitive cycling between -40°C and 85°C at 85% relative humidity;
- simulated impact of one-tenth (25mm) ball at terminal velocity;
- 2700 VDC frame/cell string isolation test;
- a "sharp heat" test, consisting of 1000 hours of exposure to 85°C and 85% relative humidity;
- a "hot-spot" test, which determines a module's ability to tolerate localized shadowing (which can cause reverse-biased operation and localized heating);
- simulated wind loading of 125 mph (200 kph).

**Mechanical Characteristics**
- **Weight:** 15.9 pounds (7.2 kg)
- **Dimensions:** Dimensions in brackets are in millimeters

![Diagram of MSX60 module](image)

**Typical Electrical Characteristics**

<table>
<thead>
<tr>
<th></th>
<th>MSX-64</th>
<th>MSX-60</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum power (Pmax)</td>
<td>64W</td>
<td>50W</td>
</tr>
<tr>
<td>Voltage @ Pmax (Vmp)</td>
<td>17.5V</td>
<td>17.1V</td>
</tr>
<tr>
<td>Current @ Pmax (Imp)</td>
<td>3.06A</td>
<td>3.5A</td>
</tr>
<tr>
<td>Guaranteed minimum Pmax</td>
<td>62W</td>
<td>58W</td>
</tr>
<tr>
<td>Short-circuit current (ISC)</td>
<td>4.0A</td>
<td>3.8A</td>
</tr>
<tr>
<td>Open-circuit voltage (Voc)</td>
<td>21.3V</td>
<td>21.1V</td>
</tr>
<tr>
<td>Temperature coefficient of open-circuit voltage</td>
<td>$-0.1 \times 10^{-3^\circ}C$</td>
<td></td>
</tr>
<tr>
<td>Temperature coefficient of short-circuit current</td>
<td>$(0.005 \pm 0.05)%^\circ C$</td>
<td></td>
</tr>
<tr>
<td>Temperature coefficient of power</td>
<td>$(0.98 \pm 0.05)%^\circ C$</td>
<td></td>
</tr>
<tr>
<td>NCC1</td>
<td>4372°C</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. These modules are tested, labeled and shipped in 12V configuration. These data represent the performance of typical 12V modules as measured in their output terminals, and do not include the effect of both individual equipment- and circuit-level testing. The data is based on measurements made at a solar simulator at Standard Test Conditions (STC), which are:
   - 1 kW/m² (1 sun) at a directivity of 1.5x,
   - cell temperature of 25°C or at otherwise specified (on curve),
   - operating characteristics may vary significantly. To determine the characteristics of modules in 6V configuration, divide the 12V voltage characteristics by 2 and multiply current characteristics by 2. Power values are unchanged.

2. Under most climatic conditions, the cells in a module operate hotter than the ambient temperature. NCC (Nominal Operating Cell Temperature) is an indication of this temperature differential. It is the cell temperature under Standard Operating Conditions (ambient temperature of 25°C, solar irradiation of 1 kW/m², and wind speed of 1 m/s).

**Download**
- **MSX-60 I-V XLS**
- **MSX-64 I-V XLS**
- **Download CAD**
Appendix B

B.1 m-file for the MPPT Model

% model of the Maximum Power Point Tracker (MPPT)

function [Vmpp,Impp,Pmax] = MPPT(Vmin, dV, Vmax,G,T)

%initialize Vmpp, Impp and Pmax

Impp = 0;
Vmpp = 0;
Pmax = 0;
for V = Vmin: dV: Vmax;
    Ia = msx60(V,G,T);
    P = Ia*V;
    if P > Pmax;
        Pmax = P;
        Vmpp = V;
        Impp = Ia;
    else
    end
end

B.2 m-file for MOSFET Power loss Model

function [Psw_on,Pon,Psw_off,Ploss] = Mosfet(Va,Ia,p,T)

% constants gm, rdson, Vt, Cgs, tr, tf
gm = 42*((T+273)/300) ^ (-2.3); % Forward Transconductance in Siemens
rdson = 0.008*((T+273)/300)^2.3 ; % static Drain-to-Source On-Resistance
Vt = 3.0 -(6*10^(-3))*T; % Gate Threshold Voltage
Cgs = 4000*10^(-12) ; % Input Capacitance in F
Cgd = 480*10^(-12); % Reverse Transfer Capacitance in F
tr = 100*10^(-9) ;% Rise Time in Sec
tf = 70*10^(-9) ;% Fall Time in Sec
Rg = 2.5; % gate resistance
%----------------------------------
Vf = Ia*rdson;
fs = 2*p*50;
t2_t1 = Rg*(Cgs+Cgd)*log ((gm*Va)/ (gm*(Va-Vt)-Ia));
Vgp = Vt + (Ia/gm);
Ig = (Va-Vgp)/Rg;
t3_t2 = (Va-Vf)*Cgd/Ig;
%----------------------------------
% losses for four transistors in a Full bridge configuration
Psw\textsubscript{on} = 2*fs*(Va*Ia*(t2\textsubscript{t1})/2 + Ia*((Va-Vf)*tr/2 + Vf*tr));

Pon = 2*Vf*Ia;

Psw\textsubscript{off} = 2*fs*(Ia*((Va-Vf)*tf/2 + Vf*tf) + Va*Ia*t3\textsubscript{t2}/2);

\%----------------------------------------

Ploss = Psw\textsubscript{on} + Pon + Psw\textsubscript{off};

\textbf{B.3 The complete Matlab Code}

1. \texttt{systemmodel}

\begin{verbatim}
home
disp ('')
disp ('Simulation Program for Grid connected PWM inverter with PV as a DC source')
disp ('')
disp ('                           By Emanuel Rashayi')
disp ('')
disp ('                           Ver 1.1, 10/03/2006')
disp ('')

Vmin = input ('Enter minimum Voltage for MPPT Algorithm :');
dV = input ('Enter the increment value for MPPT Algorithm :');
Vmax = input ('Enter the Maximum Voltage for MPPT algorithm :');
Go = input ('Enter the solar Irradiation :');
G = Go/1000;
T = input ('Enter the Ambient temperature in degC :');

[Impp, Vmpp, Pmax] = MPPTracking (Vmin, dV, Vmax, G, T);

[Vout, Iout, theta] = PWM (Impp, Vmpp);
\end{verbatim}

2. \texttt{PWM code}

\%sine PWM inverter

\begin{verbatim}function [Vout, Iout, theta] = PWM (Impp, Vmpp)
%PART I(A)
% some parameters used in the program
% p is the number of pulses per half period
dtheta = pi/500;
theta = []; vo= [];
startp = []; endp = [] ; pulsewidth = []; a=0;
\%--------------------------------------------------------------
------
fs = input('the switching frequency of the inverter(Hz)= ');
fo = input('the frequency of the output fundamental voltage(Hz)= ');
p = fs/(2*fo);
dalpha = pi/p;
w = 2*pi*fo;
W = 1/w;
\end{verbatim}
ma = input('the initial modulation index of the PWM inverter (0<ma<1) =');
Vg = input('The rms voltage of the AC bus (50Hz) =');
Np = input('The number of MXS60 modules in parallel =');
Impp = Impp*Np;
Ns = input('The number of MXS60 modules in series =');
Vmpp = Vmpp*Ns;
L = input('The inductor size of the inverter in mH: ');
L = L*10^-3;
tic

Pin = Impp*Vmpp;

%-------------------------------------------------------------------------
%PART I
%Sinusoidal variation of pulse width (deltak) with position angle (alphak)
%deltakm is the maximum pulse width
%start loop from here
%deltakm = ma*pi/p;
for k = 1:p
    alphak = (2*k-1)/(2*p)*pi;
    if(deltak >= pi/p-dtheta)
        theta1 = []; theta3 = [];
    else
        theta1 = [alphak-dalpha/2:dtheta:alphak-deltak/2];
        theta3=[alphak+deltak/2:dtheta:alphak+dalpha/2];
    end
    theta2 = [alphak-deltak/2:dtheta:alphak+deltak/2];
    startp = [startp (alphak-deltak/2)];
    endp = [endp (alphak+deltak/2)];
    pulsewidth = endp - startp;
    theta = [theta theta1 theta2 theta3 ];
    vol = Vmpp*[zeros(size(theta1)) ones(size(theta2)) zeros(size(theta3))];
    vo = [vo vo1];
end

vo = [vo -vo]; theta = W*[theta theta+pi];
disp(' startpulse(in radians)      endpulse(in radians)
pulsewidth')
    [startp'    endp'
pulsewidth']

%PART III

%Analyzing the output Voltage waveform

%Finding the rms value of the output voltage
N = length(vo);
vorms = sqrt((1/N)*sum(vo.^2));

%finding the harmonic contents of the output voltage waveform
y=fft(vo);
y(1)=[ ];
x=abs(y);
x=(sqrt(2)/N)*x;
vrms = x(1);

% using the powerflow model P = ((2*vrms*Vg)/wL)*sin(phi)
% we can approximate the load angle of maximum power transfer
phi = asin((Pin*w*L)/(2*vrms*Vg));

% Finding the THD of the output voltage
THDvo = sqrt(vorms^2-vrms^2)/vrms;

R = w*L/tan(phi);

% PART IV

% calculating the output current waveform

m = R/(w*L);
DT = dtheta;
I(1)=-10;

i=N+1:20*N;
vo(i)=vo(i-N*fix(i/N)+1);

% for i=2:20*N
%     I(i)=I(i-1)*exp(-m*DT)+vo(i-1)/R*(1-exp(-m*DT));
end

% Analysing the output current waveform
% Finding the harmonic contents of the output current waveform
for j2 = 1:N
    Io(j2) = I(j2+19*N);
    Io2 = fft(Io);
    Io2(1) = [];
    Iox = abs(Io2);
    Iox = (sqrt(2)/N)*Iox;
end

% Finding the RMS value of the output current
Iorms = sqrt(sum(Io.^2)/(length(Io)));

% PART V

% Finding the supply current waveform

for j3 = 19*N+1:20*N
    if vo(j3)~=0
        Is(j3) = abs(I(j3));
    else
        Is(j3)=0;
    end
end

% Analysing the supply current waveform
%Supply current waveform and its average value

for j4 = 1:N
    Is1(j4) = abs(Is(j4+19*N));
end

Isav = (sum(Is1)/(length(Is1)));

%Finding the THD the output current
THDIo = sqrt(Iorms^2-Iox(1)^2)/Iox(1);

disp('The rms Value of the output voltage fundamental component=')
v1rms

disp('The rms Value of the output Voltage= ')
vorms

disp('The rms value of the load current= ')
Iorms

disp('The average value of the supply current is ')
Isav

Irsms = sqrt(sum(Is1.^2)/(length(Is1)));
disp('The RMS value of the supply current is =')
Irsms

% Finding the Fourier Analysis of the supply current waveform

Is2 = fft(Is1);
Is2(1) = [];
Isx = abs(Is2);
Isx = (sqrt(2)/length(Is1))*Isx;

%PART VI
% maximum power from solar panel

disp('The load angle of the inverter in degrees = ');
phi = phi*(180/pi);
phi
disp('the voltage and maximum power point');
Vmpp
disp ('The maximum power point of the solar module')
Pin
%Displaying the calculated parameters
disp('Performance parameters are ')
THDvo = THDvo*100;
THDIo = THDIo*100;
THDvo
THDIo

%PART VII

Iout = I(19*N+1:20*N);
Vout = vo(1:N);
%Plotting the output voltage, output current, supply current, and the harmonic contents of these values

figure(1)
Is = Is(19*N+1:20*N);

subplot(3,2,1)
plot(theta,Vout,theta,a);
title('Voltage and current waveforms');
axis([0,0.02,-1.2*max(Vout),1.5*max(Vout)]);
ylabel('Output voltage/V');

subplot(3,2,2)
plot(x(1:49))
title('Harmonic Analysis');
axis([0,49,0,1.1*max(x(1:49))]);
ylabel('Von');

subplot(3,2,3)
plot(theta,Iout,theta,a);
title('');
axis([0,0.02,-1.2*max(Iout),1.5*max(Iout)]);
ylabel('Output Current/A');

subplot(3,2,4)
plot(Iox(1:49))
title('');
axis([0,49,0,1.1*max(Iox(1:49))]);
ylabel('Ion');

subplot(3,2,5)
plot(theta,Is,theta,a);
axis([0,0.02,-1.2*max(Is),1.5*max(Is)]);
ylabel('Supply Current/A');
xlabel('time/s');

subplot(3,2,6)
plot(Isx(1:49))
title('');
axis([0,49,0,1.1*max(Isx(1:49))]);
ylabel('Isn');
xlabel('Harmonic Order');
toc
Appendix C:
Hardware Design Circuits & Pictures

C.1 MOSFET DRIVER CIRCUIT

Component List:
1. MOSFET DRIVER ,IR2113 X 2
2. 2.2uF X 2
3. 4.7uF X 4
4. IN4007 X 2
5. 10R X 4
C.2 Phase shift circuit & Zero Crossing Detector

AC Voltage & Current Measurement Circuits, Zero Crossing Detector
C.3 Analogue to Digital Conversion : Interface

Analogue to Digital Conversion : Interface
C.4 SAB80C535 Microcomputer Schematic

C.5 SAB80C535 Microcomputer Board
C.6 Relay Circuit

Component List:
1. Buffers, 74LS14 X 1
2. 12 V Relay
3. 1k X 1
4. Transistor, BC548B X 1
5. Diode, IN4007 X 1
6. 39R X 1
C.7 Laboratory Prototype (Circuit Schematic)

C.8 Laboratory Prototype

A photo showing the setup for experimentation
C.9 Analysis of Current and Voltage for the DC capacitor

From the H-bridge inverter, $U_{dc}$, is the DC source and it is switched to the grid filter to create a sinusoidal current, $i_g$. We allow the duty cycle, $D$ to be $-1 \leq D \leq 1$. The average current, $i_{av}$:

$$i_{av}(t) = D(t)i_g(t) \text{..................................................eq C.9.1.}$$

and the average voltage, $U_{PWM}$:

$$U_{PWM}(t) = D(t)U_{dc} \text{..........................................eq C.9.2}$$

If pure active power is desirable, $i_g$ should be in phase with the grid voltage, $U_g$:

$$u_g(t) = \sqrt{2}U_g \sin \omega t \text{.........................................eq C.9.3}$$

$$i_g(t) = \sqrt{2}I_g \sin \omega t \text{.........................................eq C.9.4}$$

$$u_{PWM}(t) = \sqrt{2}U_{PWM} \sin(\omega t + \alpha) \text{........................................eq C.9.5}$$

From the above equations we can study the voltage and current in the DC capacitor, Figure C.9.1

Assuming that $u_c$ does not vary too much and the efficiency of the inverter is fairly high, $i_{av}$ can be expressed as:

$$i_{av}(t) = \frac{U_{PWM}(t)}{U_{dc}} i_g(t) \text{...............................................eq C.9.6}$$

But
\[ I_{mpp} U_{dc} \approx I_g U_g \]

\[
i_{sav}(t) = 2 \frac{U_{PWM}}{U_g} I_{mpp} \sin \omega t \sin(\alpha + \omega t) = \frac{U_{PWM}}{U_g} I_{mpp} \left[ \cos \alpha - \cos(2\omega t + \alpha) \right].\text{eq C.9.7}
\]

At a working point, \( U_{dc} \), the \( I_{mpp} \) of the PV source on the curve can be assumed to be linear around the working point, shown in figure C.9.2. This can be done by substituting the PV source with a voltage source, \( E \), and a resistor, \( R \), as shown. The working point is defined by \( I_{mpp} \), \( U_{dc} \) and \( R \) from the I-V curve of a specific PV.

![Diagram](image1)

**Figure C.9.2**

From figure C.9.3

\[
i_c(t) = C \frac{du_c(t)}{dt} \] \hspace{1cm} \text{eq C.9.8}

\[
i_{mpp}(t) = i_c(t) + i_{sav}(t) \] \hspace{1cm} \text{eq C.9.9}
\[ E = R i_{mp} (t) + u_c (t) \] eq C.9.10

Let \( \tau = RC \)

\[ \frac{du_c (t)}{dt} + \frac{u_c (t)}{\tau} = \frac{E}{\tau} - \frac{i_{sav} (t)}{C} \] eq C.9.11

Substituting \( i_{sav} (t) \)

\[ \frac{du_c (t)}{dt} + \frac{u_c (t)}{\tau} = \frac{E}{\tau} - \frac{I_{mp} \cdot U_{PWM}}{U_g} \left[ \cos \alpha - \cos(2 \omega t + \alpha) \right] \] eq C.9.12

The general solution to this ordinary differential equation is:

\[ u_c (t) = u_c^h (t) + u_c^p (t) \] eq C.9.13

\[ u_c^h (t) = Be^{-\frac{t}{\tau}} \]
\[ u_c^p (t) = C_1 + C_2 \sin(2 \omega t + \alpha) + C_3 \cos(2 \omega + \alpha) \]

Identifying \( C_1, C_2 \) and \( C_3 \) gives

\[ C_1 = E - I_{mp} RA \cos \alpha \]
\[ C_2 = 2 \omega \tau C_3 \]
\[ C_3 = \frac{I_{mp} RA}{1 + 2 \omega^2 \tau^2} \]

Where \( A = \frac{U_{PWM}}{U_g} \)

Where \( B \) is given by the boundary conditions at steady state

\[ u_c (0) = u_c (T) = u_c \left( \frac{\pi}{\omega} \right) \Rightarrow B = 0 \]

\[ u_c (t) = E + I_{mp} RA \left[ -\cos \alpha + \frac{2 \omega \tau}{1 + 2 \omega^2 \tau^2} \sin(2 \omega t + \alpha) + \frac{1}{1 + 2 \omega^2 \tau^2} \cos(2 \omega t + \alpha) \right] \]

eq C.9.14

To determine \( E \), we have the conditions at an average voltage:
\[ U_{dc} = \frac{1}{T} \int_{0}^{T} u_c(t) dt = E - I_{mpp} RA \cos \alpha \]

i.e. \( E = U_{dc} + I_{mpp} RA \cos \alpha \)

Finally

\[ u_c(t) = U_{dc} + \frac{I_{mpp} R U_{PWM}}{(1 + 2 \omega t^2) U_g} \left[ 2 \omega \tau \sin(2 \omega t + \alpha) + \cos(2 \omega t + \alpha) \right] \] \text{eq C.9.15}

From equation C.6.8

\[ i_c(t) = C \frac{du_c(t)}{dt} = \frac{2 \omega \tau I_{mpp} U_{PWM}}{(1 + 2 \omega t^2) U_g} \left[ 2 \omega \tau \cos(2 \omega t + \alpha) - \sin(2 \omega t + \alpha) \right] \] \text{eq C.9.16}
APPENDIX D

POWER MOSFET data sheet

IRFP064N

HexFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.
**Electrical Characteristics @ T_J = 25°C (unless otherwise specified)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>V_{BRDSS}</strong> Drain-to-Source Breakdown Voltage</td>
<td>55</td>
<td></td>
<td></td>
<td>V</td>
<td>V_{GS} = 0V, I_D = 250μA</td>
</tr>
<tr>
<td><strong>ΔV_{BRDSS}AT_J</strong> Breakdown Voltage Temp. Coefficient</td>
<td>0.087</td>
<td></td>
<td></td>
<td>V/°C</td>
<td>Reference to 25°C, I_D = 1mA</td>
</tr>
<tr>
<td><strong>R_{DS(on)}</strong> Static Drain-to-Source On-Resistance</td>
<td></td>
<td>0.008</td>
<td></td>
<td>Ω</td>
<td>V_{GS} = 10V, I_D = 50A</td>
</tr>
<tr>
<td><strong>V_{CASE}</strong> Gate Threshold Voltage</td>
<td>2.0</td>
<td>4.0</td>
<td></td>
<td>V</td>
<td>V_{GS} = V_{SS}, I_D = 250μA</td>
</tr>
<tr>
<td><strong>gs</strong> Forward Transconductance</td>
<td>42</td>
<td></td>
<td></td>
<td>S</td>
<td>V_{GS} = 25V, I_D = 50A</td>
</tr>
<tr>
<td><strong>I_{SS}</strong> Drain-to-Source Leakage Current</td>
<td></td>
<td>25</td>
<td></td>
<td>µA</td>
<td>V_{GS} = 55V, V_{DS} = 0V</td>
</tr>
<tr>
<td><strong>I_{LSS}</strong> Gate-to-Source Forward Leakage</td>
<td></td>
<td>100</td>
<td></td>
<td>nA</td>
<td>V_{GS} = 20V</td>
</tr>
<tr>
<td><strong>I_{LSS}</strong> Gate-to-Source Reverse Leakage</td>
<td></td>
<td>-100</td>
<td></td>
<td>nA</td>
<td>V_{GS} = -20V</td>
</tr>
<tr>
<td><strong>Q_g</strong> Total Gate Charge</td>
<td></td>
<td>170</td>
<td></td>
<td>nC</td>
<td>I_D = 50A</td>
</tr>
<tr>
<td><strong>Q_G</strong> Gate-to-Source Charge</td>
<td></td>
<td>32</td>
<td></td>
<td>nC</td>
<td>V_{PS} = 44V</td>
</tr>
<tr>
<td><strong>Q_GD</strong> Gate-to-Drain (&quot;Miller&quot;) Charge</td>
<td></td>
<td>74</td>
<td></td>
<td></td>
<td>V_{GS} = 10V, See Fig. 6 and 13</td>
</tr>
<tr>
<td><strong>t_{ON}</strong> Turn-On Delay Time</td>
<td></td>
<td>14</td>
<td></td>
<td>ns</td>
<td>V_{DP} = 28V</td>
</tr>
<tr>
<td><strong>t_r</strong> Rise Time</td>
<td></td>
<td>100</td>
<td></td>
<td>ms</td>
<td>I_D = 50A</td>
</tr>
<tr>
<td><strong>t_{ON}</strong> Turn-Off Delay Time</td>
<td></td>
<td>43</td>
<td></td>
<td>ns</td>
<td>R_G = 2.6Ω</td>
</tr>
<tr>
<td><strong>t_{F}</strong> Fall Time</td>
<td></td>
<td>70</td>
<td></td>
<td>ns</td>
<td>R_D = 0.3Ω, See Fig. 10</td>
</tr>
<tr>
<td><strong>I_D</strong> Internal Drain Inductance</td>
<td></td>
<td>6.0</td>
<td></td>
<td>nH</td>
<td>Between lead, 6mm (0.25in.) from package and center of die contact</td>
</tr>
<tr>
<td><strong>I_S</strong> Internal Source Inductance</td>
<td></td>
<td>13</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>C_{SS}</strong> Input Capacitance</td>
<td></td>
<td>4000</td>
<td></td>
<td>pF</td>
<td>V_{GS} = 0V</td>
</tr>
<tr>
<td><strong>C_{oss}</strong> Output Capacitance</td>
<td></td>
<td>1300</td>
<td></td>
<td>pF</td>
<td>V_{PS} = 25V</td>
</tr>
<tr>
<td><strong>C_{rss}</strong> Reverse Transfer Capacitance</td>
<td></td>
<td>400</td>
<td></td>
<td>pF</td>
<td>f = 1.0MHz, See Fig. 5</td>
</tr>
</tbody>
</table>

**Source-Drain Ratings and Characteristics**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>I_S</strong> Continuous Source Current (Body Diode)</td>
<td></td>
<td>110</td>
<td></td>
<td>Ω</td>
<td>MOSFET symbol showing the p-n junction diode</td>
</tr>
<tr>
<td><strong>I_{SM}</strong> Pulsed Source Current (Body Diode)</td>
<td></td>
<td>360</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td><strong>V_{DS}</strong> Diode Forward Voltage</td>
<td></td>
<td>1.3</td>
<td></td>
<td>V</td>
<td>T_J = 25°C, I_S = 50A, V_{GS} = 0V</td>
</tr>
<tr>
<td><strong>t_{FR}</strong> Reverse Recovery Time</td>
<td></td>
<td>110</td>
<td>170</td>
<td>ns</td>
<td>T_J = 25°C, I_S = 50A</td>
</tr>
<tr>
<td><strong>Q_{FR}</strong> Reverse Recovery Charge</td>
<td></td>
<td>450</td>
<td>680</td>
<td>nC</td>
<td>d/dt = 100A/µs</td>
</tr>
</tbody>
</table>

**Notes:**

1. Repetitive rating; pulse width limited by max. junction temperature (See fig. 11)
2. V_{DS} = 25V, starting T_J = 25°C, L = 100µH, R_D = 25Ω, I_D = 50A (See Figure 12)
3. I_{DS} ≤ 60A, d/dt ≤ 260A/µs, V_{DS} ≤ 8V, T_J ≤ 175°C
4. Pulse width ≤ 300µs; duty cycle ≤ 2%.
5. Uses IRF3205 data and test conditions
6. Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93.4
APPENDIX E

E.1 Software Routines for the SAB80C535 Microcomputer written in BASIC

'------------------------------------------------------------------------
'  (c) 2006 University of Zimbabwe, Dept of Electrical Engineering
'------------------------------------------------------------------------

'  Note : Acceptance Testing
'  file: PWMThesis06.BAS
'  Note: This program is for download to chip
'  Select 80C535.dat !!!
'  This program was developed by Mr E Rashayi
'  DATE: 06 April 2006
'  This program produces PWM signals on P1.1 and P1.2 port pins
'  It produces 25 pulses per half cycle of 50Hz(corrected using 85Hz)
'  sinusoidal signal
'  this code includes the following:
'  1. a grid synchronisation technique
'  2. Maximum power point tracking
'  3. Checking grid voltage for islanding condition
'  4. Checking DC source Voltage levels
'  5. Checking frequency deviations
'------------------------------------------------------------------------

Rem this program starts at H4100
$romstart = &H4100
Rem dimension variables
Dim V1 As Word
Dim V2 As Word
Dim C As Byte
Dim Q As Byte
Dim D2 As Byte
Dim D1 As Byte
Dim D0 As Byte
Dim Ug As Word
Dim Ig As Byte
Dim Udc As Byte
Dim Ugpk As Word
Dim Igpk As Byte
Dim Ugfreg As Byte
Dim Ugt As Byte
Dim Count As Byte
Dim Power As Byte
Dim Power0 As Byte
Dim Power1 As Byte
Dim P As Integer

Rem this program starts at H4100
$romstart = &H4100
Rem dimension variables
Dim V1 As Word
Dim V2 As Word
Dim C As Byte
Dim Q As Byte
Dim D2 As Byte
Dim D1 As Byte
Dim D0 As Byte
Dim Ug As Word
Dim Ig As Byte
Dim Udc As Byte
Dim Ugpk As Word
Dim Igpk As Byte
Dim Ugfreg As Byte
Dim Ugt As Byte
Dim Count As Byte
Dim Power As Byte
Dim Power0 As Byte
Dim Power1 As Byte
Dim P As Integer

'------------------------------------------------------------------------
'------------------------------------------------------------------------

Config Timer1 = Timer, Mode = 2 , Gate = Internal
Load Timer1 , 5
' initialisation of Maximum power point parameters
D0 = 1
D1 = 9
D2 = 5
'Making sure the inverter is shut and Deactivate the Relay Circuit
Set P5.2
Set P4.7
Set P4.6

Rem Setting Port 1 pins to LOW for no output
CLR P1.1
CLR P1.2

'Stabilizing the pulses
P = 0
Do
  Bitwait P5.1 , Reset
  Bitwait P5.1 , Set
  Incr P
Loop Until P = 500

Rem Setting Port 1 pins to LOW for no output
clr P1.1
clr P1.2
clr P4.7
clr P4.6
Rem initializing CRC and CC1 registers
Crcl = Low(65257)
Crch = High(65257)
Ccl1 = Low(65492)
Cch1 = High(65492)
Rem initialising variables: C is used as an index, Q is for quadrant of signal
C = 0

Rem enabling relevant compare registers
Ccen = &B00001000

Rem enabling the timer2 interrupt
Enable Timer2
Rem Enabling external interrupt 4
Enable Int4
Rem enabling the use of interrupts
Enable Interrupts
Rem if an interrupt occurs go this interrupt handler
On Timer2 Intsr_t2
On Int4 Fwm_sin
On Int5 Fwm_sin
Rem Setting Of Priority
Priority Set Int4 , 3
Priority Set Int5 , 2
Priority Set Timer2 , 1
Rem just to be sure the flags that Int4 & Int5 flags are cleared
clr ircon.3
clr ircon.4
Rem Configuring Timer2 control bits
T2con = &B00010001

'Activating the Relay Circuit
clr P5.2
clr P4.7
clr P4.6

'---------------------------------------------------------------------
------
Rem waiting for any interrupts
Do
'Checking grid for islanding condition

Waitms 200
Set P4.7
Set P4.6
Bitwait P5.1, Reset
Bitwait P5.1, Set
clr P4.7
clr P4.6
' MAXIMUM POWER POINT TRACKING

D2 = D0 + D1
D2 = D2 * 0.5
Gosub Pwr_in_grid
Power0 = Power
Decr D2
Gosub Pwr_in_grid
Power1 = Power
If Power1 = Power0 Then
  nop
  Delay
Else
  If Power1 > Power0 Then
    D1 = D2
  Else
    D0 = D2
  End If
End If
Loop

'---------------------------------------------------------------------
------

' SUBROUTINES

Pwr_in_grid:

'CALCULATION OF POWER INJECTED INTO THE GRID
'---------------------------------------------------------------------
------

Bitwait P5.1, Reset
Enable Timer1
On Timer1 Intsr tl
Count = 0
Start Timer1
Ug = Getad(0 , 0)
Ig = Getad(1 , 0)
Ugpk = Ug
Igpk = Ig
Do
Ug = Getad(0 , 0)
Ig = Getad(1 , 0)
If Ugpk < Ug Then
Ugpk = Ug
Else
Nop
End If
If Igpk < Ig Then
Igpk = Ig
Else
Nop
End If
Loop Until Ug = 0
Stop Timer1
Rem adjusting the calibration of the A/D converter for the grid current and voltage
Igpk = Igpk * 7
Ugpk = Ugpk * 4
Igpk = Igpk * 0.5
Power = Ugpk * Igpk
Rem Ugt = (2 * Count * 250) / 1000
Ugt = Count * 0.5
Ugfreg = 1000 / Ugt
Udc = Getad(2 , 0)
Rem adjusting the calibration of the A/D converter for the DC voltage channel
Udc = Udc * 10
If Udc > Ugpk Then
If Ugfreg > 51 Then
Gosub Switch_off
Else
If Ugfreg > 49 Then
Gosub Switch_on
Else
Gosub Switch_off
End If
End If
Else
Gosub Switch_off
End If
Return
'-----------------------------------------------------------------------
--------
Intsr_t1:
Incr Count
clr tcon.7
Return

Rem The Interrupt Handler For The Timer2 Interrupt
Intsr_t2:
Rem overflow flag cleared by software
Clr Ircon.6
Return

Switch_on:
clr P5.2
Return

Switch_off:
Set P5.2
Return

Rem The Interrupt Handler for the Int4 & Int5 Interrupts
Pwm_sin:
If P5.1 = 1 Then
    Q = 1
Else
    Q = 0
End If
Ccen = 0
clr ie.7
clr ie.5
clr ircon.3
clr ircon.4
T2con = &B00000000
If C < 23 Then
    Incr C
Else
    C = 0
    nop
    nop
End If
Select Case D2
Case 1 : V2 = Lookup(c , Dta21)
Case 2 : V2 = Lookup(c, Dta22)
Case 3 : V2 = Lookup(c, Dta23)
Case 4 : V2 = Lookup(c, Dta24)
Case 5 : V2 = Lookup(c, Dta25)
Case 6 : V2 = Lookup(c, Dta26)
Case 7 : V2 = Lookup(c, Dta27)
Case 8 : V2 = Lookup(c, Dta28)
Case 9 : V2 = Lookup(c, Dta29)
Case Else V2 = Lookup(c, Dta24)
End Select

Crl = Low(v2)
Crch = High(v2)

Select Case D2
Case 1 : V1 = Lookup(c, Dta11)
Case 2 : V1 = Lookup(c, Dta12)
Case 3 : V1 = Lookup(c, Dta13)
Case 4 : V1 = Lookup(c, Dta14)
Case 5 : V1 = Lookup(c, Dta15)
Case 6 : V1 = Lookup(c, Dta16)
Case 7 : V1 = Lookup(c, Dta17)
Case 8 : V1 = Lookup(c, Dta18)
Case 9 : V1 = Lookup(c, Dta19)
Case Else V1 = Lookup(c, Dta14)
End Select

If Q = 0 Then
Cchl = High(v1)
Ccll = Low(v1)
Ccl2 = 0
Cch2 = 0
Enable Int4
Disable Int5
Else
Cch2 = High(v1)
Ccl2 = Low(v1)
Ccll = 0
Cchl = 0
Enable Int5
Disable Int4
End If
T2con = &B00010001
Set Ie.5
Ccen = &B00101000
Set Ie.7
Return

'----------------------------------------------------------------------
--------
'LOOK UP TABLES
Rem This data table is for modulation index = 0.7
Dta11:
<table>
<thead>
<tr>
<th>Data</th>
<th>65484%</th>
<th>65484%</th>
<th>65484%</th>
<th>65465%</th>
<th>65447%</th>
<th>65430%</th>
<th>65415%</th>
<th>65402%</th>
</tr>
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<tbody>
<tr>
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<td>65382%</td>
<td>65375%</td>
<td>65372%</td>
<td>65370%</td>
<td>65372%</td>
<td>65375%</td>
<td>65382%</td>
</tr>
<tr>
<td>Data</td>
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<td>65402%</td>
<td>65415%</td>
<td>65430%</td>
<td>65447%</td>
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<td>65484%</td>
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</table>

**Dta21:**
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<th>Data</th>
<th>65412%</th>
<th>65289%</th>
<th>65290%</th>
<th>65291%</th>
<th>65291%</th>
<th>65292%</th>
<th>65293%</th>
</tr>
</thead>
<tbody>
<tr>
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<td>65295%</td>
<td>65297%</td>
<td>65298%</td>
<td>65299%</td>
<td>65300%</td>
<td>65302%</td>
</tr>
<tr>
<td>Data</td>
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<td>65304%</td>
<td>65305%</td>
<td>65306%</td>
<td>65307%</td>
<td>65308%</td>
<td>65309%</td>
</tr>
<tr>
<td>Data</td>
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<td>65310%</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

Rem: This data table is for modulation index = 0.73

**Dta22:**
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<th>Data</th>
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<th>65482%</th>
<th>65482%</th>
<th>65462%</th>
<th>65443%</th>
<th>65426%</th>
<th>65410%</th>
</tr>
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<td>65375%</td>
<td>65369%</td>
<td>65365%</td>
<td>65363%</td>
<td>65365%</td>
<td>65369%</td>
</tr>
<tr>
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<td>65426%</td>
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<td>65462%</td>
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</tr>
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**Dta23:**
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<thead>
<tr>
<th>Data</th>
<th>65412%</th>
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<th>65289%</th>
<th>65290%</th>
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<th>65292%</th>
<th>65293%</th>
</tr>
</thead>
<tbody>
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<td>65302%</td>
</tr>
<tr>
<td>Data</td>
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<td>65308%</td>
<td></td>
</tr>
<tr>
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</tr>
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Rem: This data table is for modulation index = 0.76

**Dta3:**
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<th>65480%</th>
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<th>65421%</th>
<th>65405%</th>
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<tbody>
<tr>
<td>Data</td>
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<td>65369%</td>
<td>65362%</td>
<td>65358%</td>
<td>65356%</td>
<td>65358%</td>
<td>65362%</td>
</tr>
<tr>
<td>Data</td>
<td>65369%</td>
<td>65378%</td>
<td>65390%</td>
<td>65405%</td>
<td>65421%</td>
<td>65439%</td>
<td>65459%</td>
</tr>
<tr>
<td>Data</td>
<td>65480%</td>
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</tbody>
</table>

**Dta23:**
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<tr>
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<th>65289%</th>
<th>65289%</th>
<th>65290%</th>
<th>65291%</th>
<th>65292%</th>
<th>65293%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data</td>
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<td>65295%</td>
<td>65296%</td>
<td>65298%</td>
<td>65299%</td>
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</tr>
<tr>
<td>Data</td>
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<td></td>
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</tr>
<tr>
<td>Modulation Index</td>
<td>Data 14</td>
<td>Data 24</td>
<td>Data 15</td>
<td>Data 25</td>
<td>Data 16</td>
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<tr>
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</tbody>
</table>

Rem This data table is for modulation index = 0.8

Dta14:  
Data 65455\% , 65455\% , 65455\% , 65455\% , 65434\% , 65415\% , 65398\% , 65383\% , 65370\% , 65360\% , 65353\% , 65348\% , 65347\% , 65348\% , 65353\% , 65360\% , 65370\% , 65383\% , 65398\% , 65415\% , 65434\% , 65455\% , 65455\% , 65455\% , 65455\% , 65455\% , 65455\% , 65455\% ,

Dta24:  
Data 65411\% , 65288\% , 65288\% , 65289\% , 65289\% , 65290\% , 65291\% , 65292\% , 65293\% , 65295\% , 65296\% , 65297\% , 65299\% , 65300\% , 65302\% , 65303\% , 65305\% , 65306\% , 65307\% , 65308\% , 65309\% , 65310\% , 65311\% , 65311\% , 65311\% ,

Rem This data table is for modulation index =0.82

Dta15:  
Data 65499\% , 65499\% , 65475\% , 65453\% , 65432\% , 65412\% , 65394\% , 65379\% , 65366\% , 65356\% , 65348\% , 65344\% , 65342\% , 65344\% , 65348\% , 65356\% , 65366\% , 65379\% , 65394\% , 65412\% , 65432\% , 65453\% , 65475\% , 65499\% , 65499\% , 65499\% ,

Dta25:  
Data 65411\% , 65288\% , 65288\% , 65288\% , 65289\% , 65290\% , 65291\% , 65292\% , 65293\% , 65295\% , 65296\% , 65297\% , 65299\% , 65300\% , 65302\% , 65303\% , 65305\% , 65306\% , 65307\% , 65309\% , 65310\% , 65310\% , 65311\% , 65311\% , 65312\% ,

Rem This data table is for modulation index = 0.85

Dta16:  
Data 65498\% , 65498\% , 65473\% , 65450\% , 65428\% , 65408\% , 65389\% , 65373\% , 65360\% , 65349\% , 65341\% , 65337\% , 65335\% , 65337\% , 65341\% , 65349\% , 65360\% , 65373\% , 65389\% , 65408\% , 65428\% , 65450\% , 65473\% , 65498\% , 65498\% ,

Dta26:  

- 125 -
<table>
<thead>
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<th>65288%</th>
<th>65288%</th>
<th>65288%</th>
<th>65290%</th>
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<th>65292%</th>
</tr>
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<tr>
<td>Data 65305%</td>
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<td>65310%</td>
<td>65311%</td>
<td>65311%</td>
<td>65312%</td>
</tr>
<tr>
<td>Data 65312%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

Rem This data table is for modulation index = 0.88

<table>
<thead>
<tr>
<th>Dta17: Data 65496%</th>
<th>65496%</th>
<th>65471%</th>
<th>65447%</th>
<th>65424%</th>
<th>65403%</th>
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<tr>
<td>Data 65354%</td>
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<td>65403%</td>
<td>65424%</td>
<td>65447%</td>
<td>65471%</td>
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<tr>
<td>Data 65496%</td>
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</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Dta27: Data 65411%</th>
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<th>65287%</th>
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<th>65288%</th>
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</tr>
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<td>65328%</td>
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<td>65334%</td>
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<tr>
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<td>65403%</td>
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<td>65447%</td>
<td>65471%</td>
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Rem This data table is for modulation index = 0.91

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<th>65420%</th>
<th>65399%</th>
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<tr>
<td>Data 65347%</td>
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<td>65379%</td>
<td>65399%</td>
<td>65420%</td>
<td>65444%</td>
<td>65469%</td>
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</tr>
<tr>
<td>Data 65495%</td>
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<table>
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<th>65289%</th>
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</tr>
</thead>
<tbody>
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<td>65302%</td>
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</tr>
<tr>
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<td>65310%</td>
<td>65311%</td>
<td>65311%</td>
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<tr>
<td>Data 65313%</td>
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Rem This data table is for modulation index = 0.95

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</tbody>
</table>
E.2 SAB80C535 development system

EPROM /RAM memory division

<table>
<thead>
<tr>
<th>Code memory access</th>
<th>Data Memory access</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000H 3FFFH EPROM 0000H 3FFFH</td>
<td>0000H 3FFFH</td>
</tr>
<tr>
<td>4000H 7FFFH RAM 0000H 3FFFH</td>
<td>4000H 7FFFH</td>
</tr>
<tr>
<td>8000H BFFFH EPROM 4000H 7FFFH</td>
<td>8000H BFFFH</td>
</tr>
<tr>
<td>C000H FFFFH RAM 4000H 7FFFH</td>
<td>C000H FFFFH</td>
</tr>
</tbody>
</table>

Programming the 80C535 Single Board Computer using BASCOM-8051
Source Code
This can be developed using the BASIC language in BASCOM – 8051. Program development is easy in this environment. BASCOM – 8051 compiler can produce Hex code either in INTEL format or EMON 52 format. The EMON 52 format is selected. The 80C535 single board computer has on-board EMON 52 monitor program.

V25COM
This program is used to download Hex files from a PC to the 80C535 Single Board computer using RS232. The baud rate used is 4800.
To download a hex file, first enter the name of the file after pressing Ctr F. Please note that the Hex file should be in the same folder as the V25COM application program. To start download press Ctr D.

EMON 52 Monitor Program
EMON 52 expects RAM from address 4000H onwards. The command prompt is indicated with a ‘#’. On reset the following line will be displayed.

-- EMON52 - - version 0.1 (2.7 1992) RAMTOP = 44
Any of the following commands can be used:
X, D, P, R, F and M
e.g. To run a program in RAM enter the command X 4100
X command
This is used to execute programs in memory. The syntax is always X start addr.
D command
This command is used to display data storage. The syntax is always D start addr.
P command
This command is used to display program storage. The syntax is always P start addr.
R command
This command is used to display internal Ram. The syntax is always R start addr.

F command
This command is used to fill data storage. The syntax is always F start addr. To exit from this command press X.
M command
This command is used to fill internal ram storage. The syntax is M start addr. To exit from this command press X.

E.3 SAB80C535 Monitor Program
;
; EMON52.A51
;
; Martin Ohsmann
; SMOD=1, so serial prescaler=16
; Timer auto preload=243, so divide clock by 13 gives 4807.69 Baud
;
V24SPD EQU 256-13 ; speed for V24
;
; SFR definitions
;
P5         EQU O0D0H
P1         EQU 0090H
P3         EQU 00B0H
DPL        EQU 0082H
DPH        EQU 0083H
IE         EQU 00A8H
ACC        EQU 00E0H
BCC        EQU 00F0H
SP         EQU 0081H
;
PCON       EQU 0087H
TCON       EQU 0088H
TMOD       EQU 0089H
TL1        EQU 008BH
TH1        EQU 008DH
;
SCON       EQU 0098H
SBUF       EQU 0099H
;
; Bit Definitions
;
T0     EQU 0B4H
T1     EQU 0B5H
;
; RAM Definitions
;
ORG 030H
COMMAND DS 1 ; for MON call , MUST be address 030H !!!!!!
CNT1    DS 1
HEXLEN  DS 1
INTEL1  EQU HEXLEN ; Intel record length [52]

HEXSUM  DS 2
INTELS EQU HEXSUM ; Intel checksum [52]
INTELT  EQU HEXSUM+1 ; Intel record type [52]
;
dBYTS  EQU 5 ; must be 5 , loop unrolling used 
;
dREG1  DS dBYTS
dACCU  DS dBYTS
;
; used for snapshot and MON
PSWSAV DS 1
ACCSAV DS 1
DPHSAV DS 1
DPLSAV DS 1
;
; arithmetic storage
;
top    EQU dREG1 ; overlay 2 bytes
next   EQU dREG1+2 ; overlay 2 bytes
;
FAC1   EQU top ; overlay factors for 16*16 Bit
FAC2   EQU next ; overlay
DIVI   EQU FAC2 ; overlay divisor for 32/16 bit division
QUOT   EQU FAC1 ; overlay quotient for 32/16 bit division
PROD   EQU dACCU ; overlay 5 bytes (4+ extension) for division
DIVCNT DS 1
;
Rtop   EQU $
;
;---------------------------------------------------------------------
;
ORG 0000
LJMP  START
;
; all interrupts linked via LJMP table at 4000H
;
ORG 0003H ; use jump table at address 4000H
LJMP 4003H
;
ORG 000BH
LJMP 4006H
;
;---------------------------------------------------------------------
;
- 129 -
ORG 0013H
LJMP 4009H
;
ORG 001BH
LJMP 400CH
;
ORG 0023H
LJMP 400FH
;
ORG 002BH
LJMP 4012H
;
ORG 00043H  ; new in EMON52 for 535
LJMP 4015H
;
ORG 0004BH
LJMP 4018H
;
ORG 00053H
LJMP 401BH
;
ORG 0005BH
LJMP 401EH
;
ORG 00063H
LJMP 4021H
;
ORG 0006BH
LJMP 4024H
;
ORG 00083H
LJMP 4027H
;
ORG 0009BH
LJMP 402AH
;
; compatibility with EMON51
;
ORG 100H
LJMP SND
LJMP LINK
LJMP STXT
;
; entry point for MON-CALLS
;
ORG 0200H
LJMP MON
;
; main program starts here
;
START MOV PSW,#0  ; reset register banks
MOV PCON,#080H  ; SMOD=1
MOV TMOD,#22H  ; modes are timer
MOV TH1,#V24SPD  ; preload value
MOV TL1,#V24SPD

- 130 -
SETB TCON.6 ; start counter
MOV SCON,#052H ; mode 1, Enable receiver=10H
; link interrupt procedures

MOV A,#0
MOV DPTR,#START
LCALL LINK
MOV A,#1
MOV DPTR,#INTE0
LCALL LINK
MOV A,#2
MOV DPTR,#INTF0
LCALL LINK
MOV A,#3
MOV DPTR,#INTE1
LCALL LINK
MOV A,#4
MOV DPTR,#INTF1
LCALL LINK
MOV A,#5
MOV DPTR,#INTRT
LCALL LINK
MOV A,#6
MOV DPTR,#INTF2
LCALL LINK

; [52]

MOV A,#7
MOV DPTR,#INTADC
LCALL LINK
MOV A,#8
MOV DPTR,#INTEX2
LCALL LINK
MOV A,#9
MOV DPTR,#INTEX3
LCALL LINK
MOV A,#10
MOV DPTR,#INTEX4
LCALL LINK
MOV A,#11
MOV DPTR,#INTEX5
LCALL LINK
MOV A,#12
MOV DPTR,#INTEX6
LCALL LINK
MOV A,#13
MOV DPTR,#INTRT1
LCALL LINK
MOV A,#14
MOV DPTR,#INTCTF
LCALL LINK

; test for direct TxD RxD connection
MOV R7,#0
ctST SETB P3.1
JNB P3.0,notcon ; TxD RxD not connected
CLR P3.1
JB P3.0,notcon
DJNZ R7, cTST
LJMP BEEP ; beep if direct connection

notcon SETB P3.1
JNB P3.0, UP ; test RxD connected to +5 V? if so go UP
LJMP DIALOG ; start interactive mode
UP MOV DPTR, #UPTXT
LCALL STXT
LJMP 04100H

; UPTXT DB ' LJMP TO 4100H...', 13, 10, 0
TXT0 DB 13, 10, 13, 10
DB ' --EMON52-- version 0.1 (2.7.1992) RAMTOP=', 0
ITXT1 DB ' INTERRUPT, IE0', 13, 10, 0
ITXT2 DB ' INTERRUPT, IE1', 13, 10, 0
ITXT3 DB ' INTERRUPT, TF0', 13, 10, 0
ITXT4 DB ' INTERRUPT, TF1', 13, 10, 0
ITXT5 DB ' INTERRUPT, RI/TI', 13, 10, 0
ITXT6 DB ' INTERRUPT, TF2', 13, 10, 0
; [52]
ITXT7 DB ' INTERRUPT, ADC', 13, 10, 0
ITXT8 DB ' INTERRUPT, EX2', 13, 10, 0
ITXT9 DB ' INTERRUPT, EX3', 13, 10, 0
ITXT10 DB ' INTERRUPT, EX4', 13, 10, 0
ITXT11 DB ' INTERRUPT, EX5', 13, 10, 0
ITXT12 DB ' INTERRUPT, EX6', 13, 10, 0
ITXT13 DB ' INTERRUPT, RI1/TI1', 13, 10, 0
ITXT14 DB ' INTERRUPT, CTF', 13, 10, 0

; default interrupt handlers

INTE0 MOV IE, #0 ; disable all interrupts
MOV DPTR, #ITXT1
LCALL STXT
LJMP STOP1
INTE1 MOV IE, #0 ; disable all interrupts
MOV DPTR, #ITXT2
LCALL STXT
LJMP STOP1
INTF0 MOV IE, #0 ; disable all interrupts
MOV DPTR, #ITXT3
LCALL STXT
LJMP STOP1
INTF1 MOV IE, #0 ; disable all interrupts
MOV DPTR, #ITXT4
LCALL STXT
LJMP STOP1
INTRT MOV IE, #0 ; disable all interrupts
MOV DPTR, #ITXT5
LCALL STXT
LJMP STOP1
INTF2 MOV IE, #0 ; disable all interrupts
MOV DPTR, #ITXT6
LCALL STXT
LJMP STOP1

; [52]
INTADC MOV IE,#0 ; disable all interrupts
MOV DPTR,#ITXT7
LCALL STXT
LJMP STOP1

; INTEX2 MOV IE,#0 ; disable all interrupts
MOV DPTR,#ITXT8
LCALL STXT
LJMP STOP1

; INTEX3 MOV IE,#0 ; disable all interrupts
MOV DPTR,#ITXT9
LCALL STXT
LJMP STOP1

; INTEX4 MOV IE,#0 ; disable all interrupts
MOV DPTR,#ITXT10
LCALL STXT
LJMP STOP1

; INTEX5 MOV IE,#0 ; disable all interrupts
MOV DPTR,#ITXT11
LCALL STXT
LJMP STOP1

; INTEX6 MOV IE,#0 ; disable all interrupts
MOV DPTR,#ITXT12
LCALL STXT
LJMP STOP1

; INTRT1 MOV IE,#0 ; disable all interrupts
MOV DPTR,#ITXT13
LCALL STXT
LJMP STOP1

; INTCTF MOV IE,#0 ; disable all interrupts
MOV DPTR,#ITXT14
LCALL STXT
LJMP STOP1

; STOP1 LJMP START
STOP SJMP STOP

; ---------------------------------------------------------------------------
;
; beep on P3.1
;
BEEP MOV R7,#0
LCALL BEEPL1
MOV R7,#0
LCALL BEEPL2
SJMP BEEP

; BEEPL1 SETB P3.1
LCALL BEEPT1
CLR P3.1
LCALL BEEPT1
DJNZ R7,BEEPL1
RET
;
BEEPL2 LCALL BEEPT1
LCALL BEEPT1
DJNZ R7,BEEPL2
RET
;
BEEPT1 MOV R6,#0
BEEPT2 DJNZ R6,BEEPT2
RET
;
;-----------------------------------------------
;
; interactive command interpreter
;
DIALOG MOV DPTR,#TXT0
LCALL STXT
MOV A,#Rtop
LCALL BYTE
CMND LCALL CRLF ; main interpreter loop
MOV A,'#'
LCALL SND
CMND2 LCALL GETCHR ; get command character
CJNE A,'#:',case2
LCALL INTEL
SJMP CMND2
case2 LCALL UPCASE ; and compare
CJNE A,'#X',case1
LCALL EXEC
SJMP CMND
case1 CJNE A,'#H',case0
LCALL HEXIN
SJMP CMND2
case0 CJNE A,'#D',case3
LJMP DDSP
case3 CJNE A,'#P',case4
LJMP PDSP
case4 CJNE A,'#R',case5
LJMP RDSP
case5 CJNE A,'#F',case6
LJMP FILL1
case6 CJNE A,'#M',CMND
LJMP XFILL1
;
;-----------------------------------------------
;
; Download INTEL
;
;
INTEL EQU $
MOV INTELS,#0
LCALL GET8
JC INTELe
MOV INTELL,A ; length
LCALL CHK
LCALL GET8
JC INTELe
MOV DPH,A ; address MSB
LCALL CHK
LCALL GET8
JC INTELe
MOV DPL,A ; address LSB
LCALL CHK
LCALL GET8
JC INTELe
MOV INTELt,A ; record type
LCALL CHK
MOV A,INTELt
CJNE A,#01,noendI
iCHK LCALL GET8 ; check checksum
JC INTELe
LCALL CHK
MOV A,INTELe
JNZ INTELe2
RET
noendI EQU $
CJNE A,#00,INTELe
Iloop MOV A,INTEl1 ; remaining bytes
JZ iCHK
DEC INTEl1
LCALL GET8
JC INTELe
MOVX @DPTR,A
INC DPTR
LCALL CHK
SJMP Iloop

; INTELe MOV DPTR,#INTEL0
LCALL STXT
RET

; INTELe2 MOV DPTR,#INTEL1
LCALL STXT
RET

; INTELO DB 13,10,'INTEL LOAD format ERROR !',0
INTEL1 DB 13,10,'INTEL LOAD checksum ERROR !',0
;
CHK ADD A,INTELe
MOV INTELe,A
RET

; ; fill data storage
;
FILL1 LCALL GET16 ; get start address
MOV A,R6
JNZ FILL2
LJMP CMND ; return if no hex number
FILL2 MOV DPL,R0
INC R0
MOV   DPH,@R0
FILL3 MOV   A,DPH       ; display current address
       LCALL BYTE
       MOV   A,DPL
       LCALL BYTE
       MOV   A,'#':'
       LCALL SND
       MO VX   A,DPTR      ; display current contents
       LCALL BYTE
       LCALL BLANK
       LCALL GET16        ; get new contents
       MOV   R5,A         ; save last character
       MOV   A,R6
       JNZ   FILL4        ; change if input
       CJNE  R5,#' ',FILL5
       SJMP  FILL6        ; on BLANK go on
FILL5 EQU $
       LJMP  CMND         ; exit from loop on other character
FILL4 MOV   A,@R0       ; fetch byte and store at DPTR
       MOVX  @DPTR,A
FILL6 LCALL CRLF
       INC   DPTR
       SJMP  FILL3

;-----------------------------------------------------------------------
; fill internal ram storage
;
xFILL1 LCALL GET16       ; get start address
       MOV   A,R6
       JNZ   xFILL2
       LJMP  CMND         ; exit from loop on other character
xFILL2 MOV   DPL,@R0
       INC   R0
       MOV   DPH,@R0
xFILL3 MOV   A,DPL       ; display current address
       LCALL BYTE
       MOV   A,'#':'
       LCALL SND
       MOV   R1,DPL
       MOV   A,@R1
       LCALL BYTE
       LCALL BLANK
       LCALL GET16       ; get new contents
       MOV   R5,A         ; save last character
       MOV   A,R6
       JNZ   xFILL4
       CJNE  R5,#' ',xFILL5
       SJMP  xFILL6       ; on BLANK go on
xFILL5 EQU $
       LJMP  CMND
xFILL4 MOV   R1,DPL
       MOV   A,@R0
       MOV   @R1,A
xFILL6 LCALL CRLF
       INC   DPTR
       SJMP  xFILL3
; display data storage
;
DDSP    LCALL GET16
       MOV   A,R6
       JZ    DDSP1           ; do not update DPTR if no input
       MOV   DPL,@R0
       INC   R0
       MOV   DPH,@R0
DDSP1   MOV   R3,#8
DDSP2   MOV   R2,#16
       LCALL DDMP1
       DJNZ  R3,DDSP2
       LJMP  CMND

DDMP1   LCALL CRLF
       MOV   A,DPH
       LCALL BYTE
       MOV   A,DPL
       LCALL BYTE
       MOV   A,'#':'
       LCALL SND
       LCALL BLANK
DDMPL   MOVX   A,@DPTR
       LCALL BYTE
       LCALL BLANK
       INC   DPTR
       DJNZ  R2,DDMPL
       RET

; display program storage
;
PDSP    LCALL GET16
       MOV   A,R6
       JZ    PDSP1           ; do not update DPTR if no input
       MOV   DPL,@R0
       INC   R0
       MOV   DPH,@R0
PDSP1   MOV   R3,#8
PDSP2   MOV   R2,#16
       LCALL PDMP1
       DJNZ  R3,PDSP2
       LJMP  CMND

PDMP1   LCALL CRLF
       MOV   A,DPH
       LCALL BYTE
       MOV   A,DPL
       LCALL BYTE
       LCALL BLANK
       MOV   A,'#':'
       LCALL SND
PDMPL  MOV    A,#0
MOVC   A,@A+DPTR
LCALL  BYTE
LCALL  BLANK
INC    D PTR
DJNZ   R2,PDMPL
RET

;--------------------------------------------------------------------
; display internal RAM
;
RDSP   LCALL GET16
MOV    A,R6
JZ    RDSP1          ; do not update DPTR if no input
MOV    DPL,@R0
INC    R0
MOV    DPH,@R0
RDSP1  MOV    R3,#8
RDSP2  MOV    R2,#16
LCALL  RDMP1
DJNZ   R3,RDSP2
LJMP   CM ND

; RDMP1  LCALL  CRLF
MOV    A,DPL
LCALL  BYTE
LCALL  BLANK
MOV    A,'#':'
LCALL  SND
RDMP1  MOV    R0,DPL
MOV    A,@R0
LCALL  BYTE
LCALL  BLANK
INC    D PTR
DJNZ   R2,RDMP1
RET

;--------------------------------------------------------------------
; EXEC   LCALL GET16
MOV    DPL,@R0
INC    R0
MOV    DPH,@R0
MOV    PSW,#0
MOV    R0,#0
MOV    R1,#0
MOV    R2,#0
MOV    R3,#0
MOV    R4,#0
MOV    R5,#0
MOV    R6,#0
MOV    R7,#0
MOV    BCC,#0
MOV    A,#0
JMP    @A+DPTR
ACK EQU 006H
NACK EQU 015H

HEXIN MOV A,#ACK ; acknowledge request
  LCALL SND
  LCALL GET17 ; get byte count
  MOV HEXLEN,@R0
  MOV R0,#HEXSUM ; checksum:=0
  LCALL CLR16
  LCALL GET17 ; get start address
  MOV DPL,@R0
  INC R0
  MOV DPH,@R0
  DEC R0
  hexlp LCALL GET17 ; get successive bytes
    MOV A,@R0
    MOVX @DPTR,A ; store at address
    INC DPTR
    MOV A,R0
    MOV R1,A ; exchange pointer
    MOV R0,#HEXSUM ; add value in SUM
    LCALL ADD16
    DJNZ HEXLEN,hexlp
    LCALL GET17 ; get checksum
    MOV R1,#HEXSUM
    MOV A,@R0 ; compare with computed checksum
    XRL A,@R1
    JNZ hexerr
    INC R0
    INC R1
    MOV A,@R0
    XRL A,@R1
    JNZ hexerr
  hexok MOV A,#ACK ; if ok then acknowledge
    LCALL SND
    RET
  hexerr MOV A,#NACK ; else negative acknowledge
    LCALL SND
    RET

;-----------------------------

LINK MOV R7,DPL ; target addr in DPTR; table offset in A
  MOV R6,DPH
  MOV DPTR,#4000H
  MOV BCC,#3
  MUL AB
  MOV DPL,A
  MOV A,#2 ; LJMP instruction
    MOVX @DPTR,A
    INC DPTR
    MOV A,R6
MOVX @DPTR, A
INC DPTR
MOV A, R7
MOVX @DPTR, A
RET

; function codes for MON calls
ccCHR EQU 001H
ccSTXT EQU 002H
ccBYTE EQU 003H
ccHEX16 EQU 004H
ccdRO16 EQU 005H
ccdRO32 EQU 006H
cchRO16 EQU 007H
cchRO32 EQU 008H
ccGETC EQU 010H
ccTSTC EQU 011H
ccGET16 EQU 012H
ccGET10 EQU 013H
ccGETU EQU 014H
ccSNAP EQU 020H
ccLTIME EQU 021H
ccSTIME EQU 022H
ccLINK EQU 040H
ccADD EQU 050H
ccSUB EQU 051H
ccMUL EQU 052H
ccDIV EQU 053H
ccABS EQU 054H
ccNEG EQU 055H

; main monitor service routine
MON MOV ACCSAV, A ; do not change first lines!
MOV PSWSAV, PSW
MOV A, COMMAND
ttSTIME CJNE A, #ccSTIME, ttLTIME
LCALL STIME
RET ; gives delay of

ttLTIME CJNE A, #ccLTIME, ttSNAP
LCALL LTIME
RET ; gives delay of

ttSNAP CJNE A, #ccSNAP, ttSTXT
LJMP SNAP

ttSTXT CJNE A, #ccSTXT, ttBYTE
LJMP STXT
ttBYTE CJNE A,#ccBYTE,ttCHR
MOV A,ACCSAV
LJMP BYTE

ttCHR CJNE A,#ccCHR,ttHEX16
MOV A,ACCSAV
LJMP SND

ttHEX16 CJNE A,#ccHEX16,ttdRO16
MOV A,DPH
LCALL BYTE
MOV A,DPL
LJMP BYTE

ttdRO16 CJNE A,#ccdRO16,ttdRO32
LJMP dDSP16

ttdRO32 CJNE A,#ccdRO32,tthRO16
LJMP dDSP32

tthRO16 CJNE A,#cchRO16,tthRO32
LJMP hDSP16

tthRO32 CJNE A,#cchRO32,ttGETC
LJMP hDSP32

ttGETC CJNE A,#ccGETC,ttTSTC
LJMP GETCHR

ttTSTC CJNE A,#ccTSTC,ttGET10
LJMP TSTC

ttGET10 CJNE A,#ccGET10,ttGET16
LJMP GET10

ttGET16 CJNE A,#ccGET16,ttGETU
LJMP GET16

ttGETU CJNE A,#ccGETU,ttLINK
LJMP GETUPC

ttLINK CJNE A,#ccLINK,ttADD
LJMP LINK1

ttADD CJNE A,#ccADD,ttSUB
LJMP rADD16

ttSUB CJNE A,#ccSUB,ttMUL
LJMP rSUB16

ttMUL CJNE A,#ccMUL,ttDIV
LJMP rMUL16

ttDIV CJNE A,#ccDIV,ttABS
LJMP rDIV16

ttABS CJNE A,#ccABS,ttNEG
LJMP rABS16

ttNEG CJNE A,#ccNEG,ttERR1
LJMP rNEG16

ttERR1 MOV DPTR,#ERRTXT1
LCALL STXT
LJMP 0

ERRTXT1 DB 'illegal call to MON ! ABORT',13,10,0
;
;------------------------------------------------------------------------------
--
;
; Short time delay
;
STIME MOV A,DPL ; 6+DPTR*15 microsec (MOV DPTR + CALL adds 4)
ORL A,DPH
JZ SRET1
SETB C
MOV   A, DPL
SUBB  A, #0
MOV   DPL, A
MOV   A, DPH
SUBB  A, #0
MOV   DPH, A
NOP
NOP
SJMP  STIME

SRET1   RET

; Long Time delay
;
LTIME   MOV   A, DPL      ; 6 + DPTR * (15 + TIME0) micros (MOV DPTR + CALL add 4)
   ORL   A, DPH      ; 6 + DPTR * 1000 micros
   JZ    SRET2
   SETB  C
   MOV   A, DPL
   SUBB  A, #0
   MOV   DPL, A
   MOV   A, DPH
   SUBB  A, #0
   MOV   DPH, A
   ACALL TIME0
   SJMP  LTIME

SRET2   RET

n1      EQU   196
TIME0   MOV   DPLSAV, n1      ; (n1+1) * 5 microsec = 985 micros
   NOP
TIME0L  NOP
   NOP
   NOP
   DJNZ  DPLSAV, TIME0L
   RET

;------------------------------------------------------------------------

--

LINK1   MOV   A, ACCSAV      ; restore A
   LJMP LINK            ; use old MON1 routine

;------------------------------------------------------------------------

--

SNAP    EQU $                  ; display snapshot
   MOV   DPLSAV, DPL      ; PSW and ACC have already been saved
   MOV   DPHELL, DPH
   MOV   DPTR, #SNAPTXT
   LCALL  STXT

   MOV   A, ACCSAV      ; display ACCUS
   LCALL  BYTE
   LCALL  BLANK

   MOV   A, BCC

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LCALL BYTE
LCALL BLANK

; LCALL BLANK ; PWW comes from PSWSAV
MOV A,PSWSAV
LCALL BYTE
LCALL BLANK

; LCALL BLANK ; display SP
MOV A,SP
LCALL BYTE
LCALL BLANK

; MOV A,DPHSAV ; display DPH,DPL
LCALL BYTE
MOV A,DPLSAV
LCALL BYTE
LCALL BLANK

; LCALL BLANK ; display R0 .. R7
MOV A,R0
LCALL BLANK
MOV A,R1
LCALL BLANK
MOV A,R2
LCALL BLANK
MOV A,R3
LCALL BLANK
MOV A,R4
LCALL BLANK
MOV A,R5
LCALL BLANK
MOV A,R6
LCALL BLANK
MOV A,R7
LCALL BLANK

; MOV DPH,DPHSAV
MOV DPL,DPLSAV
MOV A,ACCSAV
MOV PSW,PSWSAV

RET
SNAPTXT DB 13,10,' A  B PSW  SP DPTR R0 R1 R2 R3 R4 R5 R6 R7'
DB 13,10,0

;--------------------------------------------
--
;
; Arithmetic routines
;
rADD16 EQU $              ; @R0 + @R1 goes to top
        MOV   A,@R0
        ADD   A,@R1
        MOV   top,A
        INC   R0
        INC   R1
        MOV   A,@R0
        ADDC  A,@R1
        MOV   top+1,A
        MOV   R0,#top
        RET

rSUB16 EQU $              ; @R0 - @R1 goes to top
        CLR   C
        MOV   A,@R0
        SUBB  A,@R1
        MOV   top,A
        INC   R0
        INC   R1
        MOV   A,@R0
        SUBB  A,@R1
        MOV   top+1,A
        MOV   R0,#top
        RET

rMUL16 EQU $                 ; @R0 * @R1 goes to PROD
        MOV   FAC1+0,@R0
        MOV   FAC2+0,@R1
        INC   R0
        INC   R1
        MOV   FAC1+1,@R0
        MOV   FAC2+1,@R1
        ACALL MUL16
        MOV   R0,#PROD       ; result pointer in R0
        RET

rDIV16 MOV   PROD+0,@R0
        INC   R0
        MOV   PROD+1,@R0
        INC   R0
        MOV   PROD+2,@R0
        INC   R0
        MOV   PROD+3,@R0
        MOV   DIVI,@R1
        INC   R1
        MOV   DIVI+1,@R1
        ACALL DIV16
        MOV   R0,#QUOT       ; quotient pointer
        MOV   R1,#PROD+2    ; remainder pointer
        RET

rABS16 INC  R0              ; is ABS set CY if negative
        MOV   A,@R0
        JNB  ACC.7,nonegl
        DEC  R0
        SJMP rNEG16
noneg1 CLR C

RET

; rNEG16 MOV A,@R0 ; set negative @ R0
XRL A,#0FFH
ADD A,#1
MOV @R0,A
INC R0
MOV A,@R0
XRL A,#0FFH
ADDC A,#0
MOV @R0,A
SETB C
RET

;--------------------------------------------------------------------
;
; 32 / 16 bit division routine
;
DIV16 MOV PROD+4,#00H ; clear extension approx. 1000 microsec
MOV DIVCNT,#16      ; 15 normal steps, last step: remainder!
DIVLP ACALL SHR5
ACALL TRYSUB ; try and perform subtraction, results in CY
ACALL SHLQ ; shift CY into QUOTIENT
DJNZ DIVCNT,DIVLP
RET

;
TRYSUB EQU $
CLR C ; no borrow
MOV A,PROD+2
SUBB A,DIVI+0
MOV A,PROD+3
SUBB A,DIVI+1
MOV A,PROD+4 ; is accu extension
SUBB A,#0
JNC SUBIT
RET

SUBIT MOV A,PROD+2 ; now really subtract, we have no borrow from before
SUBB A,DIVI+0
MOV PROD+2,A
MOV A,PROD+3
SUBB A,DIVI+1
MOV PROD+3,A
MOV A,PROD+4 ; is accu extension
SUBB A,#0
MOV PROD+4,A
RET

;
SHLQ CPL C
MOV A,QUOT+0 ; use carry from before and shift into quotient
RLC A
MOV QUOT+0,A
MOV A,QUOT+1
RLC A
MOV QUOT+1,A
RET

SHR5 EQU $
CLR C ; shift 5 bytes = product+ACC 17 bit extension
MOV A,PROD+0
RLC A
MOV PROD+0,A
MOV A,PROD+1
RLC A
MOV PROD+1,A
MOV A,PROD+2
RLC A
MOV PROD+2,A
MOV A,PROD+3
RLC A
MOV PROD+3,A
MOV A,PROD+4
RET

;----------------------------------------------------------------------
--
MUL16 MOV A,FAC1+0 ; 16*16 multiply -> 32 bit ( approx. 70 microsec )
MOV BCC,FAC2+0
MUL AB ; low * low byte
MOV PROD+0,A
MOV PROD+1,BCC
MOV A,FAC1+1
MOV BCC,FAC2+1
MUL AB ; high * high byte
MOV PROD+2,A
MOV PROD+3,BCC
MOV A,FAC1+1 ; mixed prod 1
MOV BCC,FAC2+0
MUL AB
ADD A,PROD+1 ; add 3 byte wide
MOV PROD+1,A
MOV A,PROD+2
ADDC A,BCC
MOV PROD+2,A
MOV A,PROD+3
ADDC A,#0
MOV PROD+3,A
MOV A,FAC1+0 ; mixed prod 2
MOV BCC,FAC2+1
MUL AB
ADD A,PROD+1 ; add 3 byte wide
MOV PROD+1,A
MOV A,PROD+2
ADDC A,BCC
MOV PROD+2,A
MOV A,PROD+3
ADDC A,#0
MOV PROD+3, A
RET
;
;
--
;
dDSP32 EQU $ ; long 32 bit dec display of value at R0
LCALL dCNVa ; prepare conversion buffer
LCALL dCNVb ; convert 4 bytes
LCALL dCNVb
LCALL dCNVb
LCALL dCNVb
MOV R1, #dACCU+dBYTES
MOV R6, #dBYTES
LCALL dDSP2 ; display string
RET
;
hDSP32 EQU $ ; long 32 bit hex display of value at R0
INC R0
INC R0
INC R0
MOV A, @R0 ; point to most significant byte
LCALL BYTE
DEC R0
MOV A, @R0
LCALL BYTE
DEC R0
MOV A, @R0
LCALL BYTE
DEC R0
MOV A, @R0
LCALL BYTE
RET
;
hDSP16 EQU $ ; 16 bit display hexadecimal
INC R0 ; point to higher byte
MOV A, @R0
LCALL BYTE ; display
DEC R0
MOV A, @R0
LCALL BYTE ; display lower byte
RET
;
dDSP16 EQU $ ; word 16 bit dec display of value at R0
LCALL dCNVa ; prepare conversion
LCALL dCNVb ; convert two bytes
LCALL dCNVb
MOV R1, #dACCU+3
MOV R6, #3
LCALL dDSP2 ; display 3 BCD bytes so 65535 fits
RET
;
;
--
;
--
;
dCNVa MOV A, #0
MOV dACCU+0,A ; init dec conversion dACCU:=0 ; dREG1:=1
MOV dACCU+1,A
MOV dACCU+2,A
MOV dACCU+3,A
MOV dACCU+4,A
MOV dREG1+0,#1
MOV dREG1+1,A
MOV dREG1+2,A
MOV dREG1+3,A
MOV dREG1+4,A
RET
;
    dCNVb MOV A,@R0 ; convert Byte at R0 , inc R0
    INC R0
DCNVb1 MOV R2,A ; convert Byte ACC
    MOV R6,#8 ; convert R2 using dACCU and dREG1
dCNV1 MOV A,R2 ; get bit from R2
    RRC A
    MOV R2,A
    JNC dCNV2 ; if CY add dREG1 to dACCU using BCD
    dCNV2 LCALL ADD1 ; dREG1:=2*dREG1
    DJNZ R6,dCNV1 ; loop until all 8 bits done
    RET
;
    DOUBL1 MOV A,dREG1+0 ; dREG1:=2*dREG1 , BCD coded 5 bytes
    ADD A,dREG1+0
    DA A
    MOV dREG1+0,A
    MOV A,dREG1+1
    ADDC A,dREG1+1
    DA A
    MOV dREG1+1,A
    MOV A,dREG1+2
    ADDC A,dREG1+2
    DA A
    MOV dREG1+2,A
    MOV A,dREG1+3
    ADDC A,dREG1+3
    DA A
    MOV dREG1+3,A
    MOV A,dREG1+4
    ADDC A,dREG1+4
    DA A
    MOV dREG1+4,A
    RET
;
    ADD1 MOV A,dACCU+0 ; dACCU:=dACCU+dREG1 , bcd coded 5 bytes
    ADD A,dREG1+0
    DA A
    MOV dACCU+0,A
    MOV A,dACCU+1
    ADDC A,dREG1+1
    DA A
    MOV dACCU+1,A
    MOV A,dACCU+2
    ADDC A,dREG1+2
DA    A
MOV   dACCU+2,A
MOV   A,dACCU+3
ADDC  A,dREG1+3
DA    A
MOV   dACCU+3,A
MOV   A,dACCU+4
ADDC  A,dREG1+4
DA    A
MOV   dACCU+4,A
RET
;
dDSP2  NOP              ; display R6 bytes in decreasing order @R1
dDSP1p DEC  R1         ; used for decimal or hexadecimal output
    MOV   A,@R1
    LCALL BYTE
    DJNZ  R6,dDSP1p
    RET
;
;----------------------------------------------------------------------
--
;
GET8   EQU   $          ; get a Byte without ECHO
    LCALL GETHX1
    JC    err8
    RL    A
    RL    A
    RL    A
    ANL   A,#0F0H
    MOV   R7,A
    LCALL GETHX1
    JC    err8
    ORL   A,R7
    CLR   C
    RET
err8   RET
;
GET17  MOV   R0,#dACCU  ; get hex number without echo
    LCALL CLR16      ; compare with GET16
get17l LCALL GETHX1
    JNC   OK17
    MOV   R0,#dACCU
OK17:  MOV   R7,A
    LCALL SHL16      ; *16
    LCALL SHL16
    LCALL SHL16
    LCALL SHL16
    MOV   A,R7
    ADD   A,@R0
    MOV   @R0,A
    SJMP  get17l
;
GETHX1 LCALL GETUPC
    SJMP  GOON2
GETHEX LCALL GETUPC
LCALL ECHO
GOON2 CLR C
SUBB A,'0'
JC hcor1
SUBB A,#10
JNC nohex1
ADD A,#10
ISHEX CLR C
RET
nohex1 SUBB A,#7
JC hcor2
SUBB A,#6
JNC hcor3
ADD A,#16
SJMP ISHEX
nohex: SETB C
RET
hcor1 ADD A,'0'
SJMP nohex
hcor2 ADD A,'0'+17
SJMP nohex
hcor3 ADD A,'0'+17+7
SJMP nohex
;
ECHO CJNE A,#13,EC1
LCALL SND
MOV A,#10
EC1 LJMP SND
;
GET16 MOV R0,#dACCU ; get hex value into dACCU, count digits in R6
LCALL CLR16 ; value:=0
MOV A,'#H' ; send prompt
LCALL SND
MOV A,'#>'
LCALL SND
MOV R6,#0 ; count significant hex digits
get16l LCALL GETHEX ; get input character
JNC OK1 ; go on if hexadecimal
MOV R0,#dACCU ; return address of accu also
RET
OK1: INC R6 ; update number of digits
MOV R7,A ; save input value
LCALL SHL16 ; dACCU:=dACCU * 16
LCALL SHL16
LCALL SHL16
LCALL SHL16
MOV A,R7
ADD A,@R0 ; add input value (no CY)
MOV @R0,A
SJMP get16l
;
;----------------------------------------------------------------------
--
;
GET10 MOV R0,#dACCU ; get decimal value into ACCU0, digits in R6
LCALL CLR16 ; value:=0
MOV   A,'#D'     ; prompt
LCALL SND
MOV   A,'#>'
LCALL SND
MOV   R6,#0      ; significant hex digits
get10l LCALL GETDEC
JNC   OK1d       ; go on if ok
MOV   R0,#dACCU  ; return address of accu also
RET
OK1d   INC   R6         ; update digit count
MOV   R7,A       ; saves chr value
MOV   R2,dACCU   ; LSB
MOV   R3,dACCU+1 ; MSB
MOV   A,R2       ; multiply by 10 this value
MOV   BCC,#10
MUL   AB
MOV   dACCU,A
MOV   dACCU+1,BCC
MOV   A,R3
MOV   BCC,#10
MUL   AB
ADD   A,dACCU+1  ; add to old MSB
MOV   dACCU+1,A
MOV   A,R7       ; char value
ADD   A,dACCU    ; add input value
MOV   dACCU,A
MOV   A,dACCU+1
ADDC  A,#0       ; account for CY
MOV   dACCU+1,A
SJMP  get10l

GETDEC LCALL GETUPC     ; get decimal character, set CY if not
LCALL ECHO
CLR   C
SUBB  A,'#0'
JC    nodec
SUBB  A,#10
JNC   nodec
ADD   A,#10
CLR   C
RET
nodec  SETB   C
RET

;--------------------------------------------------------------------------

--

; 16 bit arithmetic for internal monitor use
; 16 bit value stored in order low,high byte
;
CLR16  MOV   @R0,#0
INC   R0
MOV   @R0,#0
DEC   R0
RET
ADD16  MOV  A,@R0      ; start at low digits
    ADD  A,@R1
    MOV  @R0,A
    INC  R0       ; increment pointers
    INC  R1
    MOV  A,@R0
    ADC  A,@R1    ; with CY from last ADD
    MOV  @R0,A
    DEC  R0       ; restore pointers
    DEC  R1
    RET

; SHL16  MOV  A,@R0      ; shift left 16 bit value
    ADD  A,@R0
    MOV  @R0,A
    INC  R0
    MOV  A,@R0
    ADC  A,@R0
    MOV  @R0,A
    DEC  R0
    RET

;------------------------------------------------------------------------
--
;
; low level IO routines
;
; STXT   EQU   $          ; send text from program store at DPTR
    MOV   A,#0       ; destroy ACC and DPTR
    MOVC  A,@A+DPTR
    JZ    ETXT
    LCALL SND
    INC   DPTR
    SJMP  STXT
ETXT   RET
;
; BLANK  MOV   A,'#'     ; send BLANK
    SJMP  SND
;
; BYTE   PUSH  ACC        ; send BYTE hexadecimal , destroy ACC only
    SWAP  A
    LCALL NIBBLE
    POP   ACC
NIBBLE  ANL   A,#0FH
    ADD  A,#246
    JC    HEXOUT
    ADD  A,#58
    SJMP  SND
HEXOUT  ADD  A,#65
    SJMP  SND
;
; CRLF   MOV   A,#13      ; send a CRLF
    LCALL SND
    MOV   A,#10
    LCALL SND
    RET
; SND   JNB  SCON.1,SND ; must not destroy any reg
CLR  SCON.1
MOV  SBUF,A
CJNE A,#10,OK2
WAITCR MOV  CNT1,#100 ; wait for slow scrolling terminals
LOP1 MOV  A,#255
LOP2 DJNZ ACC,LOP2
DJNZ CNT1,LOP1
MOV A,#10
OK2 RET
;
GETUPC LCALL GETCHR ; get upper case character from serial port
LCALL UPCASE
RET
;
UPCASE CLR C ; convert character to upper case letter
SUBB A,'#a'
JC UPC1 ; char <97 a-->0 z-->25
SUBB A,#26
JC UPC2 ; (char-a)<26, do upper case translation
ADD A,#26+'a'
RET
UPC2 ADD A,#26+'A'
RET
UPC1 ADD A,'#a'
RET
;
GETCHR EQU $ ; get character from serial port
GETC1 JNB SCON.0,GETC1
CLR SCON.0
MOV A,SBUF
RET
;
TSTC JB SCON.0,ister ; test if character present, return 1 else 0
MOV A,#0
RET
ister MOV A,#1
RET
;
;------------------------------------------------------------------------
;
END
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